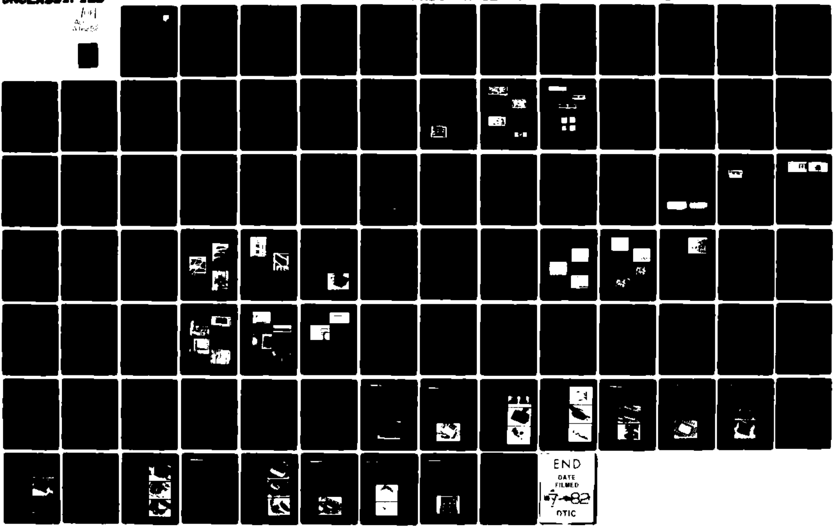
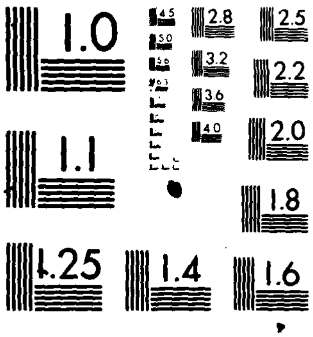
AD-A116 252   MARTIN MARIETTA AEROSPACE ORLANDO FL   F/G 9/5
QUALITY ASSURANCE PROCEDURES FOR LSI.(U)
MAR 82 L A MIRTH   F30602-79-C-0071

UNCLASSIFIED   RADC-TR-82-43   NL

1 of 1
AD
A116252



END
DATE
FILMED
7-82
DTIC


1.0
4.5
5.0
5.6
6.3
2.8
2.5
3.2
2.2
3.6
4.0
2.0
1.1
1.8
1.25
1.4
1.6

MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

(12)

AD A116252

RADC-TR-82-43
Final Technical Report
March 1982

QUALITY ASSURANCE PROCEDURES FOR LSI

Martin Marietta Corporation

Lee A. Mirth

APPROVED FOR PUBLIC RELEASE; DISTRIBUTION UNLIMITED

DTIC
S ELECTE D
JUN 30 1982
A

ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, New York 13441

DTIC FILE COPY

82 06 28 001

This report has been reviewed by the RADC Public Affairs Office (PA) and is releasable to the National Technical Information Service (NTIS). At NTIS it will be releasable to the general public, including foreign nations.

RADC-TR-82-43 has been reviewed and is approved for publication.

APPROVED: John P Farrell

JOHN P. FARRELL
Project Engineer

APPROVED:

EDMUND J. WESTCOTT
Technical Director
Reliability & Compatibility Division

FOR THE COMMANDER: John P. Huss

JOHN P. HUSS
Acting Chief, Plans Office

If your address has changed or if you wish to be removed from the RADC mailing list, or if the addressee is no longer employed by your organization, please notify RADC (RBRA) Griffiss AFB NY 13441. This will assist us in maintaining a current mailing list.

Do not return copies of this report unless contractual obligations or notices on a specific document requires that it be returned.

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER
RADC-TR-82-43

2. GOVT ACCESSION NO.
AD-A116 252

3. RECIPIENT'S CATALOG NUMBER

4. TITLE (and Subtitle)
QUALITY ASSURANCE PROCEDURES FOR LSI

5. TYPE OF REPORT & PERIOD COVERED
Final Technical Report
Jan 79 - Feb 81

6. PERFORMING ORG. REPORT NUMBER
N/A

7. AUTHOR(s)
Lee A. Mirth

8. CONTRACT OR GRANT NUMBER(s)
F30602-79-C-0071

9. PERFORMING ORGANIZATION NAME AND ADDRESS
Martin Marietta Corporation
Orlando Aerospace
P. O. Box 5837, Orlando FL 32855

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
62702F
23380153

11. CONTROLLING OFFICE NAME AND ADDRESS
Rome Air Development Center (RBRA)
Griffiss AFB NY 13441

12. REPORT DATE
March 1982

13. NUMBER OF PAGES
100

14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)
Same

15. SECURITY CLASS. (of this report)
UNCLASSIFIED

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE
N/A

16. DISTRIBUTION STATEMENT (of this Report)
Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)
Same

18. SUPPLEMENTARY NOTES
RADC Project Engineer: John P. Farrell (RBRA)

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Quality Assurance	Test Methods
Microcircuits	Process Control
Large-Scale Integration	Test Procedure
Hybrids	

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Procurement of large hermetically sealed microcircuits in small quantities was found to require a specialized quality assurance test procedure which emphasizes process control. Samples of several complex circuits were fabricated and tested under a variety of controls to determine which environmental test methods were in need of modification. Recommendations are included.

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIIFED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

EVALUATION

The objective of this study was to establish effective screening and quality assurance procedures for the test of large hermetically sealed microcircuits. Existing MIL-STD-883 test methods were reviewed for adequacy and necessity with major emphasis being placed on evaluating the applicability of in-line versus end-of-line usage of various test methods.

This effort was successfully completed by a review of the process steps and failure mechanisms associated with each major phase of microcircuit fabrication and testing and verified by a two-phase test program. As a result, test method changes that affect the testing of all microcircuits and the generation of a new test procedure for custom monolithic microcircuits are forthcoming. Existing test methods which are identified for revision are salt atmosphere, solderability, die shear and external visual. New test methods for film bondability, conductor adhesion and an alternate die shear test will be considered. .

A custom LSI test procedure will be prepared using an appendix to M38510 for the definition of general requirements and a new MIL-STD-883 test method including in line/process control, screening and quality conformance testing requirements will be generated. Vendor capability evaluation and approval documentation will be prepared as an alternate to qualification for high cost low volume microcircuit procurements.

John P Farrell
JOHN P. FARRELL
Project Engineer

DTIC
COPY
INSPECTED
2

Accession For
NTIS GRA&I ☒
DTIC TAB ☐
Unannounced ☐
Codes
Avail and/or
Dist Special
A

PREFACE

This work was funded by the Rome Air Development Center (RADC) under the provisions of contract F30602-79-C-0071 to provide a basis for revisions to screening and quality assurance procedures contained in MIL-STD-883B, Test Methods and Procedures for Microelectronics.

TABLE OF CONTENTS

Page

I. INTRODUCTION 1
  1. Investigation Purpose. 1
  2. Program Constraints. 2
  3. Anticipated Results. 2

II. EXISTING STANDARDS 3
  1. Qualification 3
    a. Industry Qualification Review. 3
      (1) Salt Atmosphere 3
      (2) Solderability 4
    b. Recent Internal Data 5
  2. Screening. 6
  3. Additional Methods Needed. 7
  4. Screening Justification Curve. 7

III. TEST SAMPLES 11
  1. Test Vehicles. 11
  2. Procurement. 16
  3. Incoming Results 17
  4. Process Controls 20
    a. Normal Process Controls. 20
    b. Additional Process Controls. 21
      (1) Thick-Film Conductor Adhesion 21
      (2) Wire Bondability. 22
      (3) Bond Strength Testing 22
      (4) Die Shear 23
  5. Preseal Testing 24

IV. EVALUATION PHASE 27
  1. Package Testing. 27
    a. Anomalies Detected 27
    b. Package Damage Criteria. 28
      (1) Method 2009, External Visual Review 28
      (2) Test Vehicles 28
      (3) Test Sequence 29
      (4) Test Results 29
      (5) External Visual Method Revision 30
  2. Substrate Testing. 31
    a. Bondability Testing. 31
    b. Hybrid Conductor Adhesion Testing. 34

PRECEDING PAGE BLANK-NOT FILMED

3. Assembly Controls 37
4. Prescreen Mechanical Tests 40
    a. Mechanical Shock 40
    b. Constant Acceleration. 43
5. Screening 44
6. Failure Analysis 45
7. Evaluation Phase Findings. 46

V. VERIFICATION PHASE 47
1. Verification Test Results. 47
2. Verification Failure Analysis. 48

VI. CONCLUSIONS AND RECOMMENDATIONS. 53

APPENDIX A VERIFICATION PLAN 57
APPENDIX B EVALUATION PHASE FAILURE ANALYSIS REPORTS 67

LIST OF FIGURES

Page

1. Screening justification curve 8
2. Multilayer hybrid in 44-pin platform package 11
3. Single-layer thick-film hybrid in 24-pin platform package . . 12
4. Thin-film hybrid in 16-pin platform package 12
5. Thin-film hybrid in 24-pin flat pack 12
6. LSI in 28-pin sidebraze ceramic 12
7. LSI in 40-pin sidebraze ceramic 13
8. LSI in 28-pin glass frit sealed ceramic 13
9. LSI in 40-pin glass frit sealed ceramic 13
10. LSI in 28- and 40-pin ceramic chip carriers 13
11. Peel test comparison 21
12. Vertical pull test 24
13. Exposed basis material 29
14. Chip into sealing glass 30
15. Sealing glass cracks at leads 31
16. Dye penetrant test results 31
17. Expected degradation of Al wire bond strength on normal Au thick film 34
18. Engelhard E-416-A intentionally fabricated with low adhesion . 35
19. ESL 8831-A intentionally fabricated with low adhesion 35
20. Engelhard E-416-A normal quality 35
21. ESL 8831-A normal quality 36
22. ESL 8831-A multilevel fabricated with low adhesion 36
23. Loss of thick-film adhesion during temperature cycling 37
24. Variation in pull strength for Al wire on Au 39
25. Al wire to Au bond strength temperature response 40
26. 3 kg, 0.3m SEC 41
27. 5 kg, 0.3m SEC 41
28. 10 kg, 0.2m SEC 41
29. 20 kg, 0.2m SEC 42
30. 30 kg, 0.1m SEC 42
31. Chip capacitor separation at 30 kg constant acceleration . . . 42
32. Ceramic chip capacitor fracture at 50 kg constant acceleration 42
33. Typical 30 kg damage 43
34. Aluminum corrosion, 40-pin CERDIP 49
35. Open circuit, 40-pin CERDIP 49
36. Displaced wire loop shorted to adjacent wire, 40-pin CERDIP . 49
37. Diffusion anomalies, electrical failure, 28-pin CERDIP 49
38. Taut bond wires not detected, 40-pin CERDIP 50
39. Solid seal blow hole, chip carrier SN 149 50
40. Leakage path, 40-pin Sidebraze, SN 124 50
41. Metallization damage, chip carrier SN 149. 50
42. Solder seal leak, 40-pin Sidebraze, SN 124 51
43. Leakage path, 40-pin Sidebraze, SN 124 51

LIST OF TABLES

Page

1. Package Characteristics - Hybrids. 14
2. Package Characteristics - LSI 15
3. Materials and Construction Analysis 16
4. Quality Conformance Tests 16
5. Preconditioning and Electrical Testing 18
6. Capacitor Screening Results 18
7. Mean Bond Strength Variation with Temperature 22
8. Function Analysis Repair Activity 25
9. Prelid Burn-In Evaluation 25
10. Package Damage Test Sequence 29
11. Leak Testing Results 30
12. Engelhard E-416-A Bondability, 0.001 Al Wire 31
13. ESL 8831-A Bondability, 0.001 Al Wire 32
14. ESL 8831-A Bondability, 0.001 Au Wire 32
15. Thin-Film Au over Kenthal Bondability, 0.001 Al Wires 33
16. Thin-Film Au over Kenthal Bondability, 0.001 Au Wires 33
17. Adhesion Test Summary 36
18. Constant Acceleration Test Results 43
19. Subplot A Normal Screening Sequence 44
20. Subplot B Short Screening Sequence 44
21. Evaluation Phase Screening Results 45
22. Verification Phase Screening Results 47

PRECEDING PAGE BLANK-NOT FILMED

SECTION I

INTRODUCTION

1. INVESTIGATION PURPOSE

The objective of this study was to develop information leading to more effective screening and quality assurance procedures for the procurement of large hermetically sealed microcircuits. Presently, such microcircuits are procured utilizing criteria originally developed for less complex devices. Because of this, the quality assurance procedures for both monolithic and hybrid microcircuits required a reexamination of their environmental and mechanical testing techniques to determine the optimum levels of non-destructive stresses and the preferred sequence of tests necessary to assure package integrity and device reliability.

Since complex custom microcircuits are frequently procured in limited quantities for military applications, RADC wished to identify environmental and mechanical tests that might more effectively be performed during the various phases of microcircuit assembly rather than as end-of-line tests. Existing procedures, when used for screening and quality assurance testing of production quantities, were thought to be time consuming, costly, and difficult to implement. The inappropriateness of some test methods to large-scale microcircuits also necessitated modifications or relaxations which raised suspicions that testing may not be adequate to obtain the required levels of reliability. Concentration on controlling processes common to several device types in the manufacturing environment offers several advantages over the classical screening approach. Some of these advantages are:

1. Determination of material incompatibilities while unit costs are low
2. Data generated are more easily related to specific failure modes and mechanisms
3. Lessened impact on program schedules by early detection of problems
4. Reduced cost of testing.

Conversely, there are some concerns over any reduction in screening arising from:

1. Unforeseen failure mechanisms not activated by process control testing

2 Damage induced to a device constituent after passing the pertinent process control gate

3 Danger of jeopardizing procedures which have been successful on past products.

2. APPROACH

A review of process steps and failure mechanisms associated with each major phase of the fabrication and test cycle for large-scale microcircuits was made through interviews with cognizant Martin Marietta personnel, a literature search, and an analysis of failure reports. These were used to further define the proposed two-phase testing program. Test vehicles were chosen which represent typical large-scale integration (LSI) microcircuits in present production. The study was divided into an Evaluation Phase, which sought to determine appropriate process controls at the preassembly, assembly, and prescreening stages; and a Verification Phase, which compared the effectiveness of the recommended procedures with the existing test requirements.

Test samples consisted of one complex LSI chip in six package types plus three hybrid circuits in different package types. All were fabricated at Martin Marietta's Microelectronics Center (MEC) using standard processes. Data generated by the controlled experimentation were supplemented by internal data generated in the normal course of production testing and product problem solving.

3. PROGRAM CONSTRAINTS

This study was limited to environmental and mechanical testing of devices in large hermetic packages. Particular test methods currently under investigation on related contracts and those judged by the contracting agency to have been amply investigated on previous studies were excluded. These excluded methods are:

1 Particle Impact Noise Detection (PIND)

2 Gas analysis

3 Rework limitations.

4. ANTICIPATED RESULTS

It was intended that the results be used to form the basis for formulating process control and lot acceptance test methods appropriate to the procurement of LSI devices (large packages) that are fabricated in small lots.

SECTION II

EXISTING STANDARDS

1. QUALIFICATION

Procedures specified in MIL-STD-883B, Methods 5005.7 and 5008, were thought to be less than optimal for qualification of LSI microcircuits and hybrids produced in small lots. This hypothesis was confirmed through a review of industry comments, Martin Marietta experience, and sample testing. A discussion of industry comments and in-house experience follows, with sample testing addressed in Section III.

a. Industry Qualification Review

It was found that environmental qualification requirements were circumvented by contractual agreements when the packaging system could not otherwise qualify or when qualification would seriously impact schedules or cost. Where the microcircuit manufacturer is part of a large system contractor, internal specifications are often utilized that may or may not be as effective as standard procedures.

Package qualification in accordance with Table IV (Group D) of either Method 5005 or 5008 received the most criticism as leading to either Type I (rejection of good material) or Type II (acceptance of defective material) errors. Specific Type I errors include test methods which may be too severe compared to the intended microcircuit application, such as the cases for salt atmosphere and solderability.

(1) Salt Atmosphere

Salt Atmosphere, Method 1009 is meant to simulate the effects of seacoast atmosphere on devices. An argument can be made that the test is too severe for devices which are to be used in more protected applications but some uncertainty is usually associated with the range of possible system locations. Of greater importance is the degree to which the test measures the devices corrosion resistance. Microcircuits may fail in the field due to corrosion in three predominant modes:

_1_ Loss of continuity of leads

_2_ Bridging of conductive material between leads or between leads and metal case

_3_ Loss of hermeticity resulting from complete penetration through or separation of package elements.

In addition, the loss of markings is also considered a failure from a maintainability viewpoint.

When the package utilizes hard glass to metal seals around the leads the evaluation of lead corrosion resistance is compromised by the normal cracking of the glass meniscus which exposes unplated lead material. This area is excluded from the present definition of lead finish such that the criterion of partially separated becomes the dominant concern. However, both the actual location of the meniscus and the interpretation of partially separated are often points of contention. In practice, the requirement may be waived or the test may be passed by chance or by taking care during the preconditioning not to crack away any meniscus glass. In either case, the qualification test does not assure that actual packages placed in field usage will not be susceptible to lead failure in highly corrosive atmospheres. In this case, no improved method of evaluation for this failure mode can be recommended since the failure mechanism is inherent in the package design feature. Changes to make the test more or less sensitive will not eliminate the failure mechanism unless the industry develops a change in the design feature.

Bridging of conductive material between isolated conductors may occur in salt atmosphere testing depending upon small potentials presented by galvanic couples. However, a more realistic test would be to utilize bias voltages typical of field usage to determine susceptibility to failure when operating in a corrosive atmosphere. The possibility of doing this in conjunction with moisture resistance testing will be discussed later.

Loss of hermeticity remains an improbable failure mechanism for modern hermetic packages operating in a salt atmosphere environment. The failure criteria for evidence of corrosion over 5 percent of any package element is not unrealistic and should be retained. Likewise, the marking integrity requirements were thought to be appropriate.

(2) Solderability

Solderability, Method 2003 is meant to verify that the treatment used in the manufacturing process to facilitate soldering is satisfactory to the extent that the present method considers only a single type of solder used under prescribed conditions, the appropriateness to the manufacturing process may be questioned. The use of leadless hermetic-chip carriers for some LSI devices produces a situation where the present test method is nonapplicable due to the lack of leads. Such packages are also often attached with solders other than Sn60/Pb40. An expansion of the test method to provide wiser applicability is suggested.

Type II errors include tests which do not represent the material or stress interface present in the actual microcircuit application:

1 Mechanical Shock, Method 2002, is applied only in the Y1 axis during qualification although Y2 or shear axes may actually be used.

2 Adhesion of Lead Finish, Method 2025, evaluates a material feature which has exhibited great variability due to Ni underplating thickness differences as well as the many types of Ni underplating used. Successful test completion once does not necessarily mean that the next plating lot will be acceptable.

b. Recent Internal Data

Martin Marietta purchases packages for microcircuits to source control documentation which specifies the qualification procedure. Microcircuits produced by the Microelectronics Center (MEC) are exclusively for use at higher levels of assembly by Martin Marietta. Typically, we do not specify salt atmosphere because we have found little correlation with use history in tactical missile systems.

Criteria for glass-to-metal seal visual inspection continues to be controversial. Satisfactory results have been achieved, but the correlation to actual leak rates remains undetermined.

Martin Marietta has found that when glass-to-metal seal visual inspection is inconclusive with regard to cracking the performance of lead fatigue followed by an unsealed package leak test provides a sufficient evaluation of the propagation potential of observed cracks. This is done to an LTPD of 10 when cracks are observed.

Analysis of materials during qualification and incoming inspection plus an analysis of process change effects is seen to be a critical area. When fabricating small lots of LSI devices, the interaction of materials is difficult to estimate when design changes are incorporated after initial qualification. In particular, it has been found dangerous to requalify only the feature changed, such as package type, in lieu of requalifying the entire device due to subtle interactions which become significant because of the larger dimensions involved as compared to MSI integrated circuits. Process controls which monitor individual features such as bond strength, die or substrate attachment, package strength, etc. in relation to the product application are preferred to the requalification procedure when small quantities are produced intermittently.

Likewise, LSI technology is involved in a shift to newer packaging techniques such as hermetic chip carriers suitable for reflow soldering to large substrates. An evaluation of the assembly stresses in such cases is necessary to determine the temperature extremes to be experienced by the chip carrier system such that temperature cycling used as a process control or for screening has a sufficient excursion.

Due to the changing technology it has become necessary for Martin Marietta to increase the emphasis placed on material and material interface analysis.

2. SCREENING

LSI circuits are particularly susceptible to failures occurring at material interfaces when subjected to thermal and mechanical stress. This is due in part to larger dimensions that result in higher stress loading due to thermal coefficient of expansion mismatch and partly to large interface areas that tend to lack uniformity. Assembly by-products and contaminants can also be more easily trapped at the interface or within the bulk of a particular constituent. Since this type of failure mechanism is often activated by thermal excursions, in particular temperature cycling, evaluations of the as-made device will fail to detect faulty processes or materials. Such failures are essentially premature wearout failures and may be manifest by a poor yield in screening or by early field failure.

Large semiconductor chips (greater than 0.200 inch square) exhibit thermal cycling failure mechanisms whether attached with eutectic or epoxy. The crystalline structure of the Si-Au eutectic has been seen to propagate dislocations and fail after temperature cycling due to thermal coefficient of expansion mismatch. Likewise a large die mounted with conductive epoxy may show unstable resistance, loss of adhesion, unstable thermal conductivity, or excessive outgassing when subjected to temperature cycling if problems exist with the material or cure schedule. In both cases, a die shear test performed as an in-line process control without thermal stressing may show good adhesion and conductivity. Because of this, a process control including thermal exposure and an alternative to die shear testing was investigated as described later.

Wire bond degradation with thermal stressing is well documented. Failures are typically due to intermetallic growth in bimetallic systems, wire annealing, and cyclic grain growth. Whereas the latter case can best be avoided through design guidelines, the former cases can be limited through off-line process controls to reduce losses at later more costly steps. Temperature cycling followed by mechanical stress in the present screening sequence can detect the most severe problems but may result in near zero yield for complex devices having many possible failure sites. The mechanical test limitations imposed by the package size may also lead to the shipping of a product with unknown bond strength that is subject to further degradation in field usage.

Process controls utilizing an off-line stress test for package seals is not as readily supportable since the per-unit cost is already high. However, where electrical testing constitutes a major portion of the unit cost, such a process control may be preferable. More extensive control of packages at the manufacturer and at incoming inspection levels beyond that specified by the present qualification procedures should be instituted. Variation in package quality, especially for large packages procured in small lots, has been a significant cause of screening failures. Conducting only an unlidded seal test is insufficient for lot acceptance since plating variations and partially cracked glass-to-metal seals have been seen to cause failure at later production steps or at screening. Each package lot should have a sample subjected to stresses representing the entire manufacturing and screening sequence prior to acceptance testing when the intended use is for a high cost circuit.

3. ADDITIONAL METHODS NEEDED

This study was to provide information to base modifications or additions to environmental and mechanical test methods for improved testing of LSI circuits and complex hybrids produced in small quantities. At the outset of the program the following areas of concern were identified:

1 Salt Atmosphere, Method 1009.2, was nonrepresentative of many applications

2 Mechanical Shock, Method 2002.2, did not apply adequate inertial stresses when run at reduced levels for large packages

3 Bond Strength, Method 2011.2, had criteria for postprocessing testing which were not utilized by Methods 5004 or 5008

4 Die Shear Strength, Method 2019.1, did not cover all sizes and ha no provision for epoxy die attach

5 No substrate attach test method was available

6 No metallization adhesion test was included for hybrids

7 No bondability test method was available for conductors

8 Package plating was not adequately addressed by existing methods

9 External Visual, Method 2009.2, required clarification of chip-ou criteria, especially for large ceramic glass frit sealed packages

10 Solderability, Method 2003.2 does not cover some new packages suc as leadless chip carriers.

Other individual tests; Temperature Cycling, Method 1010; Thermal Shock, Method 1011; Constant Acceleration, Method 2001; Moisture Resistance, Method 1004 and Lead Integrity, Method 2004 were not candidate for revision but their application within the process control and screenin sequence was to be studied.

In addition to these individual test methods, the screening sequences specified in Methods 5004 and 5008 were reviewed for effectiveness. A tendency for many LSI and complex hybrid lots to have either no rejects or nearly all rejects indicated that additional process controls should be considered in conjunction with possible changes to the screening sequence.

4. SCREENING JUSTIFICATION CURVE

To be cost effective, a screening sequence should produce sufficient rejects such that cost of the failures prevented exceeds the cost of running the tests. Included in the cost of testing is the value of good products damaged or rejected by the test methods. At the other extreme, a screening sequence should produce fewer rejects than the break-even point for the added value of the rejected units compared to the cost of performing a preventive process control. Figure 1 shows a simplified diagram of this relationship. At the extreme left, the product has a sufficiently low inherent percent of defects that no additional process control or screening test is justified. In the center region, screening dominates because the cost of failure exceeds the screening cost, which is less than the additional process control cost. To the right, the process control is dominant because the increasing yield loss has caused screening to be a more costly method of preventing field failures. In the extreme case, low screening yields would prevent product shipment and further strengthen the case for process controls.

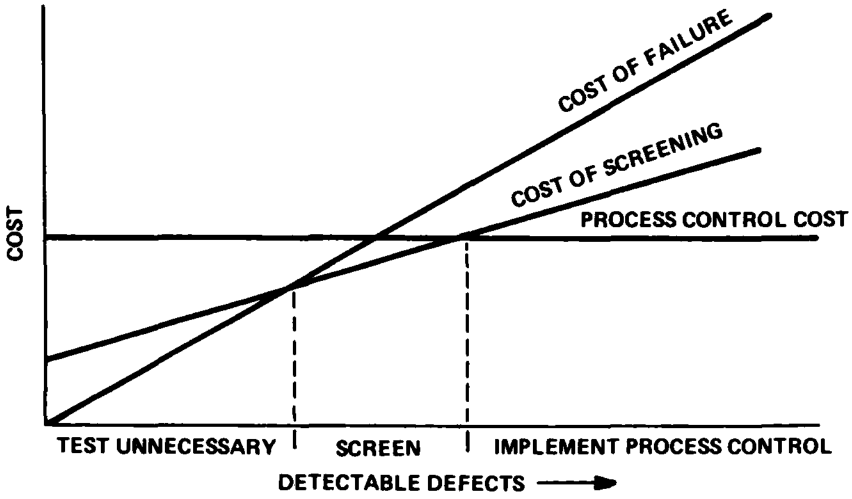


Figure 1. Screening justification curve.

This analytical technique is based on average reject rates and makes the assumption that both the screen and the process control are properly designed to detect the weakness of interest regarding possible subsequent failures. If it is found that individual lots fall almost exclusively in either the first or third region but the average is in the second region (screening dominant), a further analysis may be warranted to determine a low-cost precursor to the need to screen or to reject the entire lot.

When a screen shows a widely variant percent defective from lot to lot, it is an indication of a missing process control. For example, to protect larger hybrid packages, constant acceleration screening, Method 2001.2 was reduced to Condition B, which is capable of activating only near-zero strength bonds and component attachment. Those elements with defects which reduce the strength to as low as 20 percent of the design strength can still pass the test. However, it has been observed that an out of control process will yield a product which can be weakened by temperature exposure in the screening test to the point where most of the lot will fail under this acceleration level. In such a case, the test could be run on a sample basis with little increased risk since the percent defective distribution would be bimodal. For each lot we would conclude that either the screen was unnecessary or that the lot is unusable.

A process control which tests the attributes subject to failure during testing at later stages in the production flow can be performed on a sample basis with a low reject number (small sample). Such process control can be out-of-line (product proceeds at risk during test) when the probability of lot rejection is low. Results of such process control tests lead to a decision to accept the lot without screening, to screen the lot, or to reject the entire lot.

SECTION III

TEST SAMPLES

1. TEST VEHICLES

Test vehicles selected for this study utilized one custom LSI chip in six package types and three hybrid devices in different package types. All were fabricated by Martin Marietta's MEC using semiconductor chips purchased from other companies. Part fabrication took place in two phases, Evaluation and Verification, with approximately 50 percent of the parts built in each phase. Selection of test vehicles was based in part on devices typical of the industry at the outset of the contract.

An industry survey determined that packages with more than 40 pins were uncommon for custom LSI devices; thus it was decided that three styles of packages with 28 and 40 pins would be representative of custom LSI. Styles selected were the standard co-fired multilayer side braze, the ceramic glass frit, and the ceramic chip carrier. To minimize variables arising from electrical characteristics of the active chip, a single Martin Marietta-designed LSI was selected.

Hybrids selected represented thin-film, thick-film single layer, and thick-film multilayer technologies. Packages were 24 lead flat pack, 24 lead platform, and 44 lead platform such as is common in the industry. All utilized hard glass-to-metal seals around the leads. Figures 2 through 10 show the unlidded packages and circuits included in this study. Tables 1 and 2 give the primary structural characteristics.

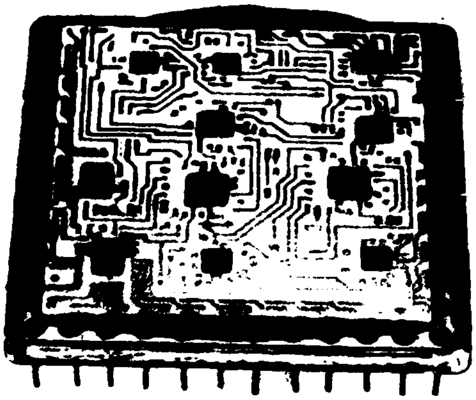


Figure 2. Multilayer hybrid in 44-pin platform package.

PRECEDING PAGE BLANK-NOT FILMED

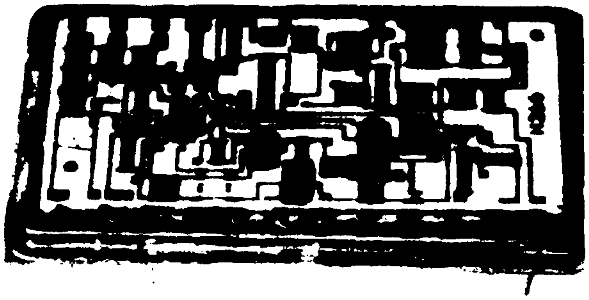
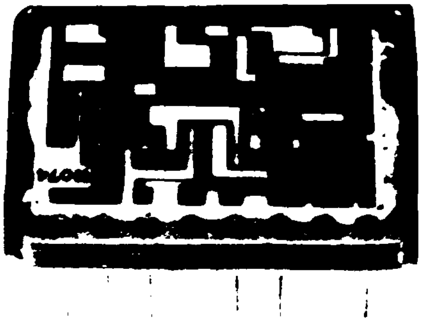


Figure 3. Single-layer thick-film hybrid in 24-pin platform package.

Figure 4. Thin-film hybrid in 16-pin platform package.



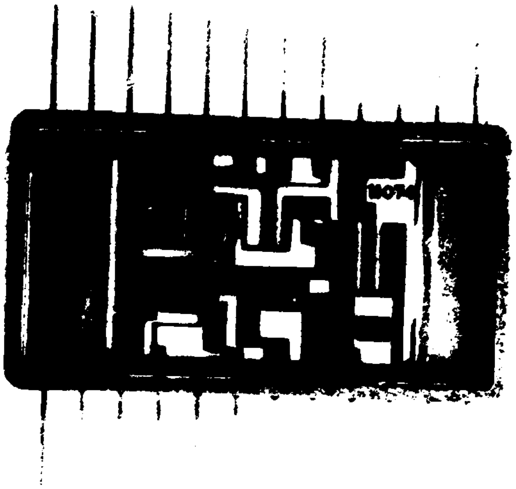


Figure 5. Thin-film hybrid in 24-pin flat pack.

Figure 6. LSI in 28-pin sidebraze ceramic.

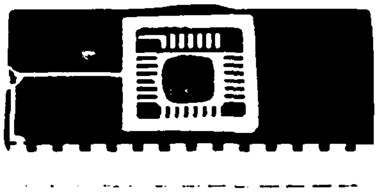
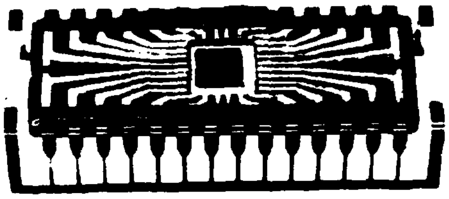


Figure 7. LSI in 40-pin sidebraze ceramic.

Figure 8. LSI in 28-pin glass frit sealed ceramic.



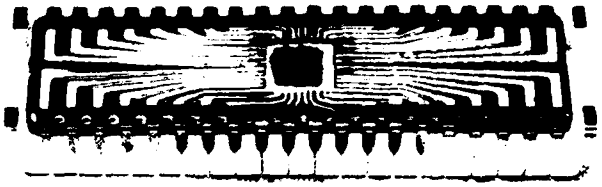


Figure 9. LSI in 40-pin glass frit sealed ceramic.

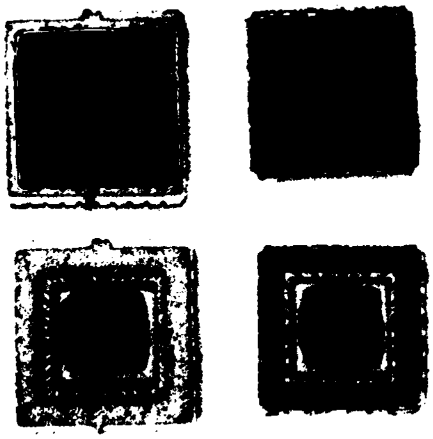


Figure 10. LSI in 28- and 40-pin ceramic chip carriers.

TABLE 1. PACKAGE CHARACTERISTICS - HYBRIDS

TYPE CONSTRUCTION	PLATFORM	PLATFORM	PLATFORM	FLATPACK
No. Pins	44	24	16	24
Plating, Header	Ni/Au	Ni/Au	Ni/Au	Ni/Au
Plating, Lid	Ni/Au	Ni	Ni	Ni/Au
Inner Seal Perimeter	4.75	3.93	3.13	3.71
Header Thickness	0.060	0.060	0.060	0.020
Lid Thickness	0.010	0.010	0.010	0.015
Sidewall Thickness	0.010	0.010	0.010	0.040
Cavity Length	1.185	1.270	0.870	1.215
Cavity Width	1.185	0.695	0.695	0.640
Cavity Height	0.160	0.124	0.124	0.110
Pin Centers	0.100			
Seal Material	One shot weld			Au/Sn
Header Material	Kovar	Kovar	Kovar	Kovar
Lid Material	CRS	CRS	CRS	Kovar
Lead Finish	Au	Au	Au	Au
Overall Length	1.270	1.370	0.970	1.295
Overall Width	1.270	0.795	0.795	0.720

TABLE 2. PACKAGE CHARACTERISTICS - LSI

TYPE CONSTRUCTION	MULTILAYER SIDE BRAZE	MULTILAYER SIDE BRAZE	CERDIP	CERDIP	HERMETIC CHIP CARRIER	HERMETIC CHIP CARRIER
No. Pins	28	40	28	40	28	40
Die Pad	Au	Au	Au	Au	Au	Au
Plating, Lid	Au	Au	n/a	n/a	Au	Au
Inner Seal/Perimeter	1.60	1.60	1.00	1.04	1.14	1.20
Body Thickness	0.080	0.080	0.077	0.077	0.045	0.060
Lid Thickness	0.010	0.010	0.060	0.050	0.010	0.010
Sidewall Thickness (Min)	0.100	0.100	0.060	0.060	0.057	0.065
Cavity Length	0.40	0.40	0.25	0.26	0.235	0.250
Cavity Width	0.40	0.40	0.25	0.25	0.235	0.250
Cavity Height	0.070	0.070	0.055	0.055	0.030	0.045
Pin Centers	0.100	0.100	0.100	0.100	0.050	0.050
Seal Material	Au/Sn Solder	Au/Sn Solder	Glass Frit	Glass Frit	Au/Sn Solder	Au/Sn Solder
Body Material	Alumina	Alumina	Alumina	Alumina	Alumina	Alumina
Lid Material	CRS	CRS	Alumina	Alumina	CRS	CRS
Lead Finish	Au	Au	Sn/Pb	Sn/Pb	Au	Au
Overall Length	1.40	2.00	1.45	2.05	0.40	0.46
Overall Width	0.60	0.60	0.52	0.52	0.40	0.46

To provide a broader representation of industry practices, the type of bond wire (Au or Al) and the method of die attach were varied on selected samples. An attempt to induce failures by adjustment of production parameters to out-of-tolerance conditions was only partially successful. It is theorized that the experienced operators, trained to maximize yields, compensated for substandard material and equipment out of adjustment. It has been suggested that use of inexperienced operators would have produced more weak parts and increased the statistical significance of the test data. Since a low number of failures is a common problem with reliability experiments, it was decided early in the program to supplement the data with experience from the microelectronics production area which produces many similar parts. Although variation in process controls was not possible for such data, thorough failure analysis information could be obtained and in many cases an improvement to a process control could be suggested by the failure cause.

2. PROCUREMENT

Packages and materials for the test samples were purchased to Martin Marietta specifications since no military specifications are available for large hybrid packages, substrates, and semiconductor chips. After acceptance through quality control testing, some additional testing was done to characterize the packages as shown in Table 3.

TABLE 3. MATERIALS AND CONSTRUCTION ANALYSIS

Solderability	Method 2003, 260°C + 10°C
Salt atmosphere	Method 1009, Condition A except 3.1
Hermeticity	Method 1014, Condition A, Unsealed
Lead fatigue	Method 2004, Condition B2
Physical dimensions	Method 2016
Insulation resistance	Method 302, Condition B, MIL-STD-202
Air bake	450°C, 5 minutes
Visual	Method 2009, except allow discoloration on nongold surfaces

Quality conformance sampling was done on each lot using the tests listed in Table 4.

TABLE 4. QUALITY CONFORMANCE TESTS

Physical dimensions	Method 2016
Insulation resistance	Method 302, Condition B, MIL-STD-202
Hermeticity	Method 1014, Condition A, Unsealed
Materials and construction	Analysis
Lead fatigue	Method 2004, Condition B2
Air bake	450°C, 5 minutes
Visual	Method 2009, except allow discoloration on nongold surfaces

Semiconductor chips for the hybrid devices were subjected to a visual examination in accordance with vendor die maps and the provisions of MIL-STD-883, Method 2010 or MIL-STD-750, Method 2072 or 2073, as applicable. Samples were taken from each lot, mounted in multilayer ceramic side braze packages with temporary epoxy attached lids, and subjected to automated testing of dc, functional, and ac parameters. Die lot acceptance was based on the results of this electrical testing. The LSI chips were custom devices procured in wafer form. After a cursory low magnification of the entire wafer, 20 die were selected on each wafer for examination in accordance with Method 2010. Location of each die to be examined is determined from a pattern for each circuit type such that a sample is obtained from each section of the wafer with weighting toward the center. Acceptance is by wafer rather than by wafer lot with the acceptance criteria based on the complexity of the circuit and the technology used by the manufacturer. Acceptance numbers range from 6 to 17 for circuits presently being procured. After initial acceptance, wafers were sent to wafer probe where units failing dc parameters were inked out. Following die separation (diamond sawing), a sample of the good die was mounted and tested to estimate the wafer lot yield. Traceability to the wafer lot was maintained in the stockroom up through the time of issue to fabrication.

Passive chips (ceramic capacitors) were inspected visually and received no further testing except for the three lots discussed below. No chip resistor was used.

Materials for thick-film screening were tested for printability by a standard use test which included patterns for conductivity/resistivity. These materials were drawn from stocks used for normal production on hybrids for various projects and thus were typical of standard products.

3. INCOMING RESULTS

All semiconductor chips were found to meet the visual and electrical specifications.

Package samples passed all tests, with the exception of the 44-pin platform package which exhibited gold plating flaking when subjected to MIL-STD-883D, Method 2004.3, Lead Integrity. Since this is not a failure criterion under this method, the anomaly was recorded and the packages released for the test samples. The leads on this package are not normally formed or bent during testing or device usage, and no evidence of flaking was exhibited in subsequent testing.

In response to a proposed revision of MIL-STD-883B, Method 5008, which called for 100 percent screening of passive chips used in Class B hybrids, a special test was run on three types of ceramic chip capacitors. As suggested by the proposed revision, the sequence presented in Table 5 was run on part of the lot. The balance of each lot remained as received to act as a control group. Table 6 offers capacitor screening results.

TABLE 5. PRECONDITIONING AND ELECTRICAL TESTING

Type	Source	Quantity	Capacitance
2BR050S472KD	Veradyne	30	4700 pF, 10%
2BR050S103KD	Veradyne	60	0.01 μF, 10%
W050FH104KG	Centralab	30	0.1 μF, 10%

1 Thermal Shock, MIL-C-15681B, para. 4.7.11 (MIL-STD-202, Method 107, Cond. A except 125°C in step 3. Unmounted, pre- and post test measurements not applicable.)

2 Voltage Conditioning, MIL-C-15681B, para. 4.7.3 100V, 125 +4, -0°C, 100 ±4h

3 Electrical Parameters

• Dielectric Withstanding Voltage	124V min.
• Insulation Resistance at 25°C	
- 2BR050S472KD	11.75 MΩ min.
- 2BR050S103KD	25 MΩ min.
- W050FH104KG	100 MΩ min.
• Capacitance	nominal ±10%
• Dissipation factor	2.5% max.

TABLE 6. CAPACITOR SCREENING RESULTS

Type	Pass/Fail	Failure Mode
2BR050S472KD	20/30	5 failed capacitance, 2 failed dissipation factor, 3 failed both
2BR050S103KD	1/60	59 failed capacitance
W050FH104KG	30/30	0 failed

Subsequent usage of these part types showed no difference between the control lots and the screened components after hybrid screening. Cost of performing this test was high since fixturing was necessary and small chips were difficult to handle unmounted. Taken as a gross average, 57.5 percent of the devices failed. Individually, 33, 98, and 0 percent of the three test lots failed.

Starting with the premise that a cost-effective screen should remove a small percentage of the lot (usually less than 25 percent) and that a screen which removes no part does not improve the average lot quality, it appears that the above screening procedure was not cost effective. If, in fact, those parts failing the screening sequence represented impending hybrid failures, a lot rejection based on a sampling plan would have been preferable. However, since none of the capacitors in the balance of the lots led to failure of their hybrid circuits during hybrid level screening, the efficiency of the test sequence is questionable.

Screening efficiency is defined as the impending failures removed divided by the impending failures in the lot minus the false removals divided by the potential false removals in the lot (good devices):

$$E_S = \frac{\gamma_R}{\gamma_I} - \frac{f_R}{f_P}$$

where:

E_S is screening efficiency
γ_R are impending failures removed
γ_I are total impending failures
f_R are false removals
f_P are potential false removals (lot size $-\gamma_I$).

If we estimate the actual values of γ_I and f_P from the performance of an unscreened sublot, we can obtain an estimate of E_S. In this case the estimate of γ_I is zero, so that the first term is undefined, thus set to zero by definition. The estimated efficiencies where +1.0 is the most efficient and -1.0 is the least efficient are as follows:

Sublot		Estimated Efficiencies
A	=	$0 - \frac{10}{30} = -0.33$
B	=	$0 - \frac{59}{60} = -0.98$
C	=	$0 - \frac{0}{30} = 0$

These estimates must be qualified by the recognition that no field use data were included in the impending failures estimates and that the electrical stress level at the component level during hybrid screening was less than the stress during component screening. In fact, the dielectric strength test at 250 percent rated voltage may be particularly inappropriate for capacitors that are applied at less than 50 percent of rated voltage and isolated from transients. In this regard, it is interesting to note the dependence of the screening efficiency calculations on the actual component application.

Sampling of passive devices to an LTPD of 10 is suggested as an efficient material control procedure with the provision that failing lots may be 100 percent screened at the option of the device manufacturer. Under LTPD sampling as defined in MIL-M-38510 we would be 90 percent confident that a lot having 10 percent defective will not be accepted on a single sample assuming the measured parameters have normal distributions. In the case where the population distribution of percent defective by lot is bimodal with maximums near zero and above 25 percent, the discrimination of an LTPD test at the 10 percent level will be improved.

4. PROCESS CONTROLS

a. Normal Process Controls

Normal process controls were supplemented with additional measurements during processing to assess the need for additional requirements within MIL-STD-883. Normal process controls were:

Test	Method	Requirement
Die Shear	2019.1	LTPD=15 each shift for each type of attachment (eutectic or epoxy).
Bond Strength	2011.2	LTPD=15 every 4 hours plus every change in materials (wire or header) for each bonder.

For hybrid devices, process controls begin with substrate preparation:

Test	Method	Requirement
Thick/thin film adhesion	Undocumented	No evidence of lift when scotch tape is applied and peeled.
Bondability	2011.2	LTDP=15 each material change.
Substrate Attach	2011, Cond. B, Y1 Unsealed	LTDP=15 each material change.
Die Shear	2019.1	LTPD=15 each shift for each type of attachment (eutectic or epoxy).
Bond Strength	2011.2	LTPD=15 every 4 hours plus every change in materials (wire or substrate network) for each bonder.

In each case, tests are conducted on as-made constituents which have not received electrical, thermal, or mechanical stress.

b. Additional Process Controls

An investigation was made to determine effective process controls which could supplement or replace the normal screening tests. It was noted that temperature exposure (particularly cyclic) is of prime importance in activating failure mechanisms associated with the process control criteria.

(1) Thick-Film Conductor Adhesion

Material manufacturers data sheets for conductor pastes generally show a reduction in adhesion of approximately 40 percent after exposure to 150°C for 1000 hours. This characteristic, adhesion stability, is a function of the specific material chosen but is also somewhat dependent on processing. An additional variable is introduced if the design includes solder attachment of components since the leaching of the gold within the conductor by the tin in the solder will increase the amount and rate of adhesion reduction. Solder leaching was observed both during the solder reflow operation and the subsequent exposure of screening tests.

Failure modes resulting from the loss of adhesion include open circuits at solder attach points and component liftoff. Although an off-line temperature cycling test of a completed substrate could be performed prior to adhesion testing, it would not indicate the effects of the component attach media and the stress due to thermal cofficient of expansion mismatch.

The scratch appearance test was suggested as a quick method of evaluating as-fired adhesion, but it is no more quantitative then the tape peel test, involving peeling a piece of cellophane tape from the conductor pattern followed by a visual examination. The normal tape test is particularly difficult to evaluate quantitatively since the actual force applied to the metallization is a function of how much the backing materials spread the force as well as of the adhesive used. Figure 11 diagrams the areas of uncertainty even if the vertical force is controlled. The worst case is obtained when the tape reaches the edge of metallization.

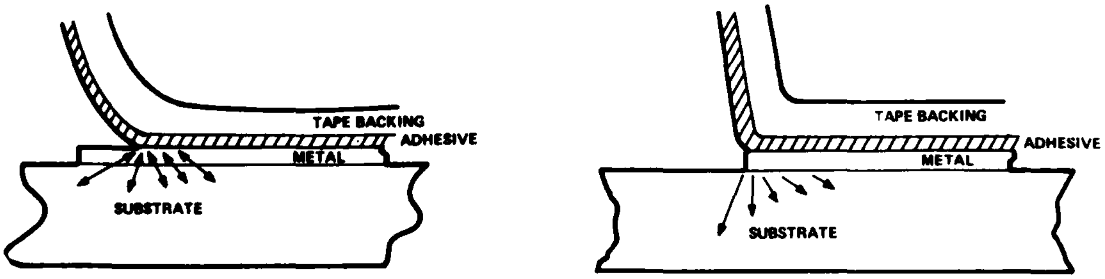


Figure 11. Peel test comparison.

A similar situation exists for application of the tape test to thin film, except that there is less spreading of the force within the metal at the line of peel, so most of the spreading is provided by the backing material.

(2) Wire Bondability

The ability to achieve a high strength wire bond is of concern on the hybrid metallizations, package pins, and semiconductor die. Since a number of geometric irregularities, surface conditions, and contaminants can reduce bondability, the most accepted procedure is to perform a process use test, i.e., bond a sample using the same procedures and equipment as in actual use and subject the sample to high temperature prior to destructive bond pull testing. Two areas are suggested for such a test in the overall process. Preassembly or substrate acceptance is a convenient location for such a test to verify compatibility of materials and processes. Bond strength testing can also be accomplished out-of-line during assembly.

(3) Bond Strength Testing

Both gold and aluminum wire bonds are affected by temperature exposure. The growth of intermetallic components at high temperatures wherever a bimetallic system is present is well documented. The annealing of the wire also has the effect of reducing the strength at the bonding site and porous plating may also act to reduce bond strength when exposed to high temperatures. Table 7 shows the results of exposing acceptable bonds to temperatures ranging from 150 to 300°C for 4 hours prior to destructive bond pull testing has been suggested by Martin Marietta's internal data and by others in the industry. Practical considerations include the possibility of the lot proceeding at risk during the test time and the need for an accurate test vehicle when the actual assembly contains materials with lower temperature limitations.

TABLE 7. MEAN BOND STRENGTH VARIATION WITH TEMPERATURE

Temperature	Time, Minutes						Hours	
°C	10	20	30	60	120	240	24	72
150	--	--	10	9.5	9.4	8.5	--	8.0
200	9.7	--	8.7	8.4	--	6.7	6.4	--
250	8.9	7.7	7.2	6.7	6.2	--	--	--
300	7.0	6.5	6.3	6.0	5.7	--	--	--

Note: Initial mean bond strength was 10.3 gram

Processing a small lot at risk while a sample is being evaluated for the wire bond's ability to withstand temperature exposure would not be a condition conducive to rework if the sample failed. Failure of the sample test would, however, prevent accumulating any additional test expense on a lot likely to have a high fallout during screening. Conversely, passing such a test may obviate the need for certain mechanical screening stresses which check for weak bonds. A high temperature destructive sample test in conjunction with a 100-percent nondestructive bond pull test as made would provide high assurance that the wire bonding system is reliable. Data taken during this study indicate that a shift in the distribution should be expected following high temperature exposure but that the dispersion remains the same or decreases. Therefore, if the sample after a temperature exposure test is sufficient to estimate the shift in the mean, and a 100-percent nondestructive test is used to limit the lower end of the original range, an estimate of the lowest strength expected from the actual circuits after equivalent temperature stress may be made. As an example, consider the 250°C data entry in Table 5 in conjunction with the actual lot which was 100-percent nondestructively tested to 2.0-gram force prior to temperature exposure in accordance with Method 2023.1.

The 1.0-mil aluminum wire bonds were loops on Au-plated headers with approximately 40-mil spans; both bonds were at equal heights. Initial strength distribution had a mean ($\overline{X}$) of 10.3g and a standard deviation (s) of 1.9g. A sample of 24 loops exposed to 250°C for 2 hours showed $\overline{X}_1$ = 6.2g and S_1 = 1.6g. This reduction in strength of 40 percent is what is expected from the annealing of the wire.

Test results from the evaluation phase combined with internal data indicate that an accelerated temperature equivalent to one hour at 300°C using an activation energy of 1.0 eV is sufficient to identify inadequate bonds. The shortening of the test time from four hours to one hour is made appropriate by the tendency for bond degradation to be bimodal with the faulty bonds degrading rapidly in comparison to the slower degradation of nominal bonds. After temperature exposure, the minimum bond strength should meet the post-seal levels of Method 2011.

(4) Die Shear

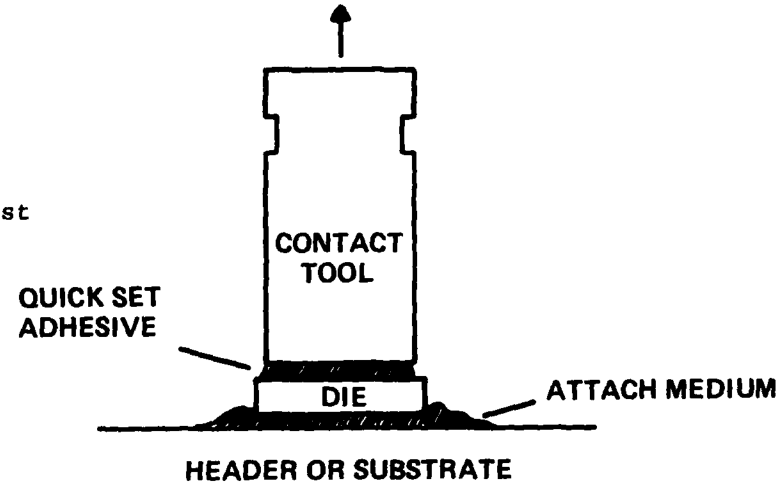
The present die shear test method (Die Shear Strength, Method 2019.1) provides criteria which vary with die attach area over the range of 22 to 80 mils square with constant shear force criteria out to 92 mils square. The failure criteria therein mix the requirement for strength with that for thermal or electrical conductivity, requiring greater force levels for dice showing less evidence of adhesion. Since this test method makes no allowance for attachment medium run up on the side of the die, there is an implication that epoxy die attach was not considered. In the case of epoxy attach with material above the bottom surface of the die on all four sides, a possibility exists that a die having no liftoff strength would be able to survive the lateral die shear force.

A vertical force exerted on the die by use of a vacuum collate such as is used for eutectic die attachment is a function of die size and pressure differential. If a compliant material is used, a pressure differential of approximately 13 psi is not unreasonable.

For a die 200 mils on a side, a vertical force of approximately 235 grams (0.52 pound) could be achieved by such a nondestructive test. A die 80 mils on a side would experience a vertical force of only 37 grams under these conditions which does not compare favorably with the 2.5-kilogram minimum shear force requirement for a die 80 mils on a side in the present test method. Assuming a die thickness of 10 mils, a 30,000g constant acceleration test would exert approximately 450 and 72 grams force on a die 200 mils square and 80 mils square, respectively. In either case, a die with adhesion over a small percentage of its total area could pass the test and have adequate mechanical strength for the application environmental but could have insufficient thermal conductivity or unexpected temperature gradients across the die which could reduce electrical performance design margins.

An alternative test method was developed based on a destructive vertical force using a simple tool and a quick curing contact adhesive. Disposable tools used were either rods or bars having a cross sectional area of 50 to 75 percent of the area of the die to be tested. A small amount of Eastman 910 was applied to the face of the tool which was then held in contact with the die surface until cured. The test is diagramed in Figure 12. Such adhesive will reach a tensile strength of 2000 psi within four hours when properly applied (including attention to shelf life and contamination). Pull testing performed perpendicular to the plane of the adhesion can exert 1000 to 1500 psi on the die attachment depending on the ratio of the tool to die area. A tool with 50 percent of the area of a die 200 mils square and an adhesive strength of 2000 psi would exert a potential force on the die bond of 18 kilograms (40 pounds) baring fracture of the silicon.

Figure 12. Vertical Pull Test



5. PRESEAL TESTING

Preseal testing effectiveness for hybrids was evaluated by electrical test only and full unsealed burn-in under nitrogen atmosphere. Preseal electrical testing will be referred to as functional analysis since it is the point in the process where all parameters, with the possible exception of certain ac or high frequency parameters, can be tested and where repair is most feasible. Although handling damage can be a problem in both cases, the functional analysis can become a standard portion of the process such that little damage is incurred. Also, since functional analysis is a "test and fix" operation, most damage can be efficiently repaired at that point.

Functional analysis consisted of placing a temporary lid on the hybrid and retaining it with an elastic band. The parts were plugged into a test socket and tested to the full functional part specification. Those failing are subjected to electrical troubleshooting followed by an internal visual inspection prior to the repair activity. Repair activity for the three hybrid types during the evaluation phase build is shown in Table 8. As an experimental variable, no functional analysis was done on similar parts during the verification phase, which showed higher fallout during screening.

TABLE 8. FUNCTION ANALYSIS REPAIR ACTIVITY

Type	Lot Size	Preseal Repairs	Screening Electrical Rejects
H266	45	5	0
H074	50	8	4
72310026	52	14	1
Totals	147	27	5

Prelid burn-in was found to be ineffective for the type of circuit utilized. Of the sample submitted, seven units out of 45 were repaired as a result of functional analysis prior to burn-in, and no failures were experienced in prelid burn-in or in the balance of either screening sequence which followed. A control group of 20 hybrids screened to a standard sequence experienced two units repaired in functional analysis and one failure during burn-in. Table 9 summarizes these data for the H266, thick-film hybrid in a 24-pin platform package. Wirebounds were half-Al and half-Au, 0.001-inch wire. Two types of gold metallization were used, and wire bonds were 100-percent nondestructively pull tested to 1.7-gram force for Al and 1.9-gram force for Au. Following prelid burn-in, pull tests were repeated at levels of 1.5g and 1.9g for Al and Au, respectively. No wire bonds failed nondestructive testing.

TABLE 9. PRELID BURN-IN EVALUATION

Test Sequence	Group I		Group II	
	ESL, AU	EH, Al	ESL, AU	EH, Al
Functional Analysis	1/11	2/12	2/11	2/11
Prelid Reverse Bias BI; 68 hours, 125°C; Dry Nitrogen Atmosphere	0/11	0/12	0/11	0/11

TABLE 9. (CONTINUED)

Test Sequence	Group I ESL, AU	Group I EH, Al	Group II ESL, AU	Group II EH, Al
Temperature Cycle	0/11	0/12		
Constant Acceleration	0/11	0/12		
Electrical	0/11	0/12		
Reverse Bias Burn-In, 100 hours	0/11	0/12	0/11	0/11
Hermeticity	0/11	0/12	0/11	0/11
Final electricals	0/11	0/12	0/11	0/11

While these data are not extensive enough to make a statistically valid statement on the virtues of prelid burn-in, they do reflect the normal experience by Martin Marietta when prelid burn-in has been required. In each case, functional analysis detected enough failures prior to seal to make the testing worthwhile (Martin Marietta normally does not delid and repair hybrids failing during sealed screening tests), while no benefit is evident from prelid burn-in. Such results indicate that the total distribution of early life failures from all mechanisms is not a smooth monotonic function; rather it seems to be bimodal with many initial defeats which are either nonoperational as built and fail immediately upon the application of power, or are weak parts subject to failure under stress in a short time at high temperature. Depending on the particular failure mechanism, such parts may have a higher probability of failure during the last 80 hours of burn-in than during the first 80 hours, thus reducing the effectiveness of a prelid burn-in. Since this issue has been studied under other contracts and was not a primary objective of this contract, no further preseal burn-in was conducted. This agrees with a previous RADC report dealing more extensively with this topic. Indications are that preseal burn-in should be reserved for cases where specific early life failure mechanisms have been identified as problems. As reported in section IV, the functional analysis was continued throughout the Evaluation Phase.

SECTION IV

EVALUATION PHASE

The Evaluation Phase of the study was intended to examine the major phases of a fabrication and test cycle with respect to the requirements of MIL-STD-883 and normal company procedures to determine how the intent of the requirements could be met in a more cost-effective manner for limited production lots of custom large-scale microcircuits. Four areas were considered for investigation: preassembly material acceptablility, assembly processing, prescreen (usually preseal) testing, and screening tests. The major tenet of this investigation was that detection of defects or substandard material could be accomplished prior to package sealing in a more cost-effective manner.

1. PACKAGE TESTING

a. Anomalies Detected

The only package anomaly found on the units procured for this contract concerned loss of gold adhesion on the leads of the 44-pin platform package when subjected to Lead Integrity, Method 2004.2, Condition B2, Lead Fatigue. (Method 2004.3 was not promulgated at the time of package procurement.) In addition to the requirements of this test method, internal Martin Marietta procedures require platform package leads to be treated as semiflexible leads and subjected to a force sufficient to cause a bend through a 30-degree arc. Failure criteria include evidence of breakage, loosening or relative motion between the terminal and the device body, plus any evidence of plating defects. This requirement is similar to that found in Method 2009.3, External Visual, Failure Criteria, 3.1(c).

This anomaly was noted and the parts accepted for the purposes of this investigation although they would not be acceptable for deliverable hardware. Examination of the packages following screening failed to show evidence of this anomaly even though the packages had been through several insertions in assembly fixtures and test sockets. Data gathered from other programs indicates that in addition to the testing defined by Method 2004, the evaluation of package plating after exposure to high temperature is important. Inspection in accordance with Method 2009 following exposure to 450°C for 5 minutes has been found effective in detecting abnormal plating. Discoloration is not a rejection criteria. Such testing should be done in addition to Group D package related tests.

Depending on the package sealing method, surface flatness was found to be a critical parameter which was not always met by the package manufacturer. Excessive camber on sealing rings combined with marginal camber of package lids produced poor yields when the packages were sealed by solder reflow. Procurement drawing dimensions were tightened to prevent a tolerance build-up situation and measurement of this dimension was shifted from a periodic requirement to a lot acceptance requirement with an LTPD=15 for packages which would experience this sealing technique. This inspection should be done for selected package types to supplement the Group D package related seal test.

b. Package Damage Criteria

(1) Method 2009 External Visual Review

A review of the inspection criteria as applicable to ceramic packages indicated that the chip-out provisions were not adequate for CERDIP (glass frit sealed ceramic dual in-line packages) styles. Since various areas of the packages have differing criticality, a single criterion of chip size results in an excessively stringent inspection.

The intent of part level test methods is that parts contained in final assemblies be free of quality defects and early life reliability defects. When considering package damage, some persons in the industry have suggested that the allowable damage should be apportioned between the unmounted device and the device after incorporation in the final assembly. Such an argument is similar to allowing degraded electrical performance following device burn-in which would be a major departure from present MIL-STD-883 philosophy. One could argue that we do allow degraded electrical performance for some devices after higher level assembly if they work in the circuit. However, this is only due to a loss of ability to fully test the devices after mounting. After assembly, we do have a similar inability to fully inspect the devices visually depending on the mounting method. The above concern with inspectability is magnified in the case of package damage to hermetically sealed devices since assemblies cannot be submitted to fine leak testing and there is no other nondestructive indication of seal degradation.

MIL-STD-883 and MIL-M-38510 define the requirements for a device which is acceptable for the application. If a particular user recognizes that his assembly processing results in device degradation, it is his responsibility to improve his processes or to select a device with higher strength.

(2) Test Vehicles

An evaluation of package damage due to chip-outs was conducted by exposing three groups of devices to environmental stresses followed by hermeticity testing. Devices had defects typical of those found during final assembly visual inspection:

1 Lot A, 30 pieces, AMD25S05, 24-pin, CERDIP with defects found at incoming inspection

2 Lot B, 50 pieces, LM747, 14-pin, side braze, assembled by Martin Marietta, 25 with chips and 25 good devices as controls

3 Lot C, 30 pieces, assorted part numbers and vendors, 14-, 16-, and 24-pin, CERDIP as removed from assembly area prior to board insertion Lots A and C were provided by Westinghouse Baltimore from their normal Quality Control system specifically for this study. Lots A and B were electrically tested prior to environmental stressing.

(3) Test Sequence

The test sequence is shown in Table 10.

TABLE 10. PACKAGE DAMAGE TEST SEQUENCE

Description	K Method Condition
Fine and gross leak	1014, Condition B and C
Thermal shock	1011, Condition B 15 Cycles
Temperature cycling	1010, Condition C, 100 Cycles
Moisture resistance	1004
Electricals, Lots A, B	Device specification
Fine and gross leak	1014, condition B and C

This sequence subjected the packages to thermal stresses which could be expected to propogate cracks existing in the area of the chip-out.

(4) Test Results

Although several Lot C devices had chips into the seal area which exposed lead frame basis material, no corrosion was observed on any of the devices. This was attributed to the low efficiency of the moisture resistance test in activating corrosion since neither chemical contaminants nor electrical bias were present. Notwithstanding the lack of corrosion, these parts are considered unacceptable for use in equipment even if not discovered until after board mounting (Figure 13).

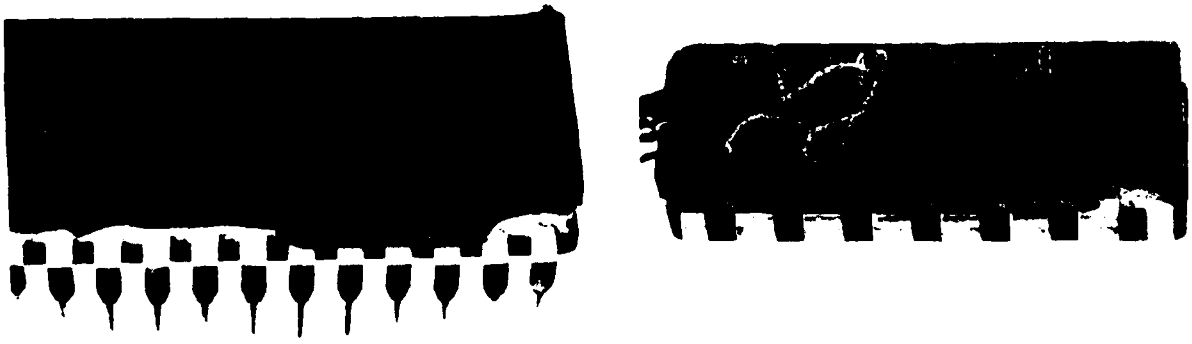


Figure 13. Exposed basis material.

Lots A and C contained samples with chip-outs extending into the CERDIP glass seal. Figure 14 shows typical seal damage. Test results showed a low correlation between chip severity and Radiflo leak rate. Leak testing using Method 1014, Conditions B and C, produced the final hermeticity tests result shown in Table 11.

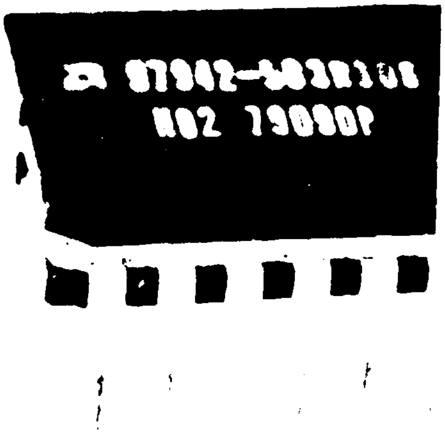


Figure 14. Chip into sealing glass.

TABLE 11. LEAK TESTING RESULTS

	Lot A		Lot C		Total
	Devices	Leakers	Devices	Leakers	(%)
Chips into seal	17	3	22	10	33
Cracks in seal	3	3	1	0	75
Chips not into seal	7	3	8	2	33
No chips or cracks	3	0	0	0	0

Devices showing cracked seals were classified as handling damage or failures occurring during testing since the cracks were not evident during the initial visual inspection. Visual inspection for cracked CERDIP seals on mounted devices appears to be of equal or greater importance than the chip-out criteria. Figure 15 is typical of the seal cracks observed. Figure 16 results from the dye penetrant test showing the path to the cavity. None of the damaged devices in Lot B failed hermeticity or showed evidence or corrosion. One undamaged device in the control group failed the final Radiflo leak test. Chip-outs which exposed metallization were classified as rejectable at the system level since they would be susceptible to attack by contaminants in the presence of moisture. No evidence of delamination was found.

(5) External Visual Method Revision

A new chip-out criterion was formulated and included in recommendations for revisions of Method 2009.

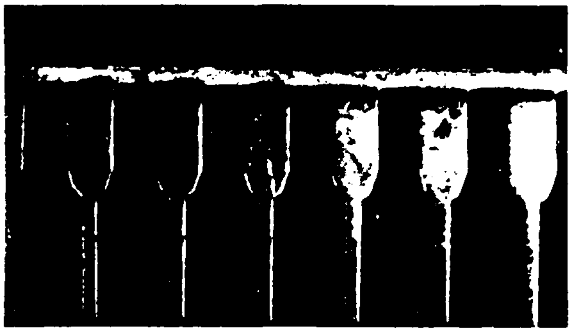


Figure 15. Sealing glass cracks at leads.

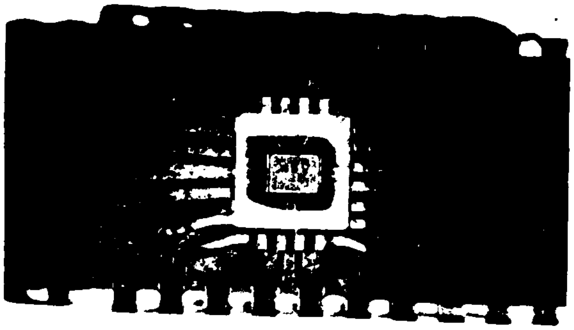


Figure 16. Dye penetrant test results.

2. SUBSTRATE TESTING

In hybrid assemblies, the basic properties of the conductive pattern on the substrate determine the finished part strength limitations with regard to bondability and adhesion. Lack of standardization of thick-film paste manufacturing and control plus the criticality of processing for both thin- and thick-film conductors results in a reasonable probability of variation in bondability and adhesion.

In addition to a measure of bondability and adhesion in the as-made parts, measurement of the degradation in properties as a result of subsequent processing, testing, and use is important.

a. Bondability Testing

Two types of thick-film gold plus one thin-film gold were used in fabricating four varieties of patterned substrates. Wire bonding was then done using both Au and Al wire by thermosonic and ultrasonic means, respectively. All work was done on semiautomatic equipment using experienced operators. Results of these tests are shown in Tables 12 through 16. All samples were drawn from lots that were later used in assembling test hybrids. As noted in the headings, some substrates were intentionally fabricated with nonstandard processing to reduce bondability.

TABLE 12. ENGELHARD E-416-A BONDABILITY, 0.001 Al WIRE

	Group	$\bar{X}$ gt	R gt	% Zero	% < 1.5 gt, NDPT
Initial	A	1.81	0.2/7.5	13	
150°C, 24 hour					
w/o NDPT	B	6.35	1.4/8.4	0	
with NDPT	C	1.27	0.1/3.4	0	24
150°C, 140 hour					
w/o NDPT	D	4.47	0.4/6.9	0	
with NDPT	E	4.09	1.6/7.1	0	0 1.5 and 0.9 gt

Notes:

Group A represents as-made **nondestructive** pull test bonds
Group B and D did not receive nondestructive pull testing (NDPT)
Group C received NDPT prior to first temperature exposure
Group E received NDPT prior to both temperature exposures
Groups A and C were intentionally overbonded to produce weak bonds
All thick film was printed thicker than normal and not cleaned prior to bonding

TABLE 13. ESL 8831-A BONDABILITY, 0.001 Al WIRE

	Group	$\overline{X}$ gf	R gf	% Zero	% < 1.5 gf, NDPT
Initial	A	2.74	0.2/7.5	10	
150°C 24 hour					
w/o NDPT	B	6.31	3.9/8.6	0	
with NDPT	C	1.96	0.6/4.8	0	30
150°C, 140 hour					
w/o NDPT	D	2.95	0.7/5.5	0	
with NDPT	E	2.95	0.2/4.5	0	0 1.5 and 0.9 gf

Notes:

- Group A represents as-made nondestructive pull test bonds
- Group B and D did not receive NDPT
- Group C received NDPT prior to first temperature exposure
- Group E received NDPT prior to both temperature exposures
- Groups A and C were intentionally overbonded to produce weak bonds
- All thick film was printed thicker than normal and not cleaned prior to bonding

It can be observed that both Groups A and C showed a high percentage of weak bonds which could have been cause for lot rejection either on the basis of percent defective allowable (PDA) for this single parameter or on the basis of a low mean pull stength as determined by the destructive testing. Conversely, the bonds that were initially made with good strength, even though the metallization was substandard, Groups D and E maintained reasonable strength even after 164 hours at 150°C. The percentage of decrease between 24 and 164 hours is more than anticipated in the latter group, and the lowest reading as indicated by the range is unacceptable after 164 hours at 150°C. This decrease in strength beyond the 40 percent expected from annealing of the Al wire can be attributed to the bimetallic overbonded system forming excessive intermetallics. Figure 17 shows normal degradation of Al wire on gold thick film of normal quality.

TABLE 14. ESL 8831-A BONDABILITY, 0.001 Au WIRE

	Group	$\overline{X}$ gf	R gf	% Zero	% < 3 gf, NDPT
Initial	A	7.43	5.2/9.2	2 at 0.1	
150°C, 24 hour					
w/o NDPT	B	7.80	6.2/8.9	0	
with NDPT	C	7.85	4.1/10.8	0	0
150°C, 140 hour					
w/o NDPT	D	7.33	5.5/9.8	0	
with NDPT	E	7.10	5.0/9.6	0	0 3.0 and 1.5 gf

Notes:

Group A represents as made nondestructive pull test bonds
Groups B and D did not receive NDPT
Group C received NDPT prior to first temperature exposure
Group E received NDPT prior to both temperature exposures
NA
All thick film was printed thicker than normal and not cleaned prior to bonding

Since wire bonds for these samples were made between metallization bonding pods, Table 14 represents an all-Au system. As could be expected, there is little change between the initial readings and any of those made subsequently.

TABLE 15. THIN-FILM AU OVER RESISTOR MATERIAL (KENTHAL) BONDABILITY, 0.001 Al WIRES

	$\bar{X}$ gf	R gf	Comments
Initial	7.5	0.2/14.3	
150°C, 160 hours	4.6	0.2/8.2	2 bonds had zero strength

TABLE 16. THIN-FILM AU OVER RESISTOR MATERIAL (KENTHAL) BONDABILITY, 0.001 AU WIRES

	$\bar{X}$ gf	R gf	Comments
Initial	7.63	5.6/9.7	Remainder passed 3 gf NDPT
150°C, 160 hours	8.58	5.7/10.4	No zero strength bonds

Thin-film substrates used for the H074 hybrid were baselined with respect to both Au and Al bonding. Substrates for these data were normal quality samples drawn from lots that were later used in hybrid assembly.

Thick film conductor adhesion should be evaluated in relation to the actual application. Due to the interaction between the conductor and solders, the adhesion test requirements should be more severe for devices using solder chip attachment than for those using polymeric or eutectic chip attachment.

When chip components are to be attached by soldering, the adhesion should be verified by soldering a wire to a bonding pad of typical dimensions and pulling vertically. This pull test should be done after temperature exposure which simulates normal assembly processing and screening. In the more prevalent case where passive components are to be attached with epoxy, the pull wire should be epoxied to the bonding pad.

Selection of the minimum adhesion criteria is dependent on the device design and the materials used. As-fired thick film conductors exhibit peel strengths ranging from 600 to 1600 psi when using a 100 mil square test pad. Depending on the material, this strength may be reduced by 30 to 60 percent after 100 hours at 150°C.

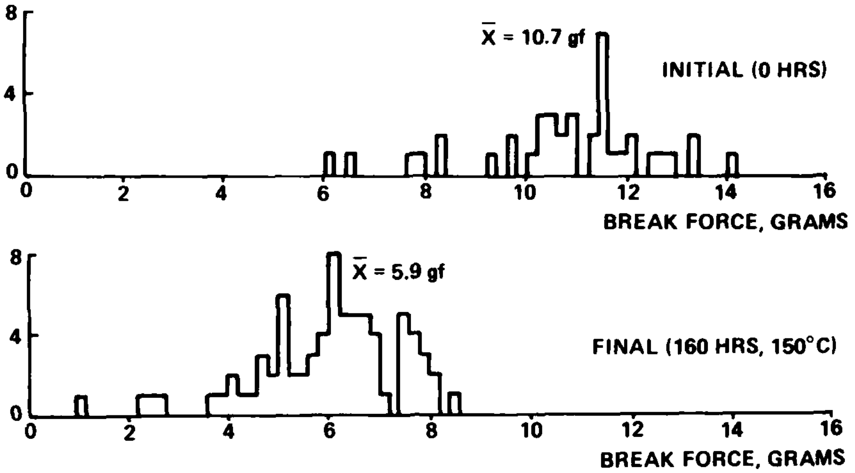


Figure 17. Expected degradation of Al wire bond strength on normal Au thick film.

The 39-percent decrease in mean bond strength in Figure 17 is attributed to the expected annealing of the aluminum. Since this gold thin-film system is not normally suitable for Al ultrasonic bonding, the wide dispersion of bond strengths is also expected and desired to produce a strength distribution appropriate to evaluate mechanical stress tests. The Au wire bond strengths shown in Table 16 are representative of normal product.

b. Hybrid Conductor Adhesion Testing

Adhesion testing was performed using thick-film substrates which were intentionally fired below the normal temperatures to produce some devices having marginal adhesion. Since there is no standard test method for adhesion, two possible methods were used. In the first test, 0.002 Au wire loops were attached and destructively pull tested to determine failure modes. A lifted metallization indicated faulty adhesion, whereas a failure elsewhere showed a minimum adhesion strength to have been attained. In the second test a sharp stylus was drawn across the metallization with sufficient force to cut the metallization when holding the stylus at right angles to the substrate. Examples are shown in Figures 18 through 22.

Table 17 summarizes the results of an attempt to provide a low-cost test which could be performed as a process control. Although not conclusive, there is an indication that thick-film metallization which has a tendency to flake rather than smear will also have a lower adhesion.

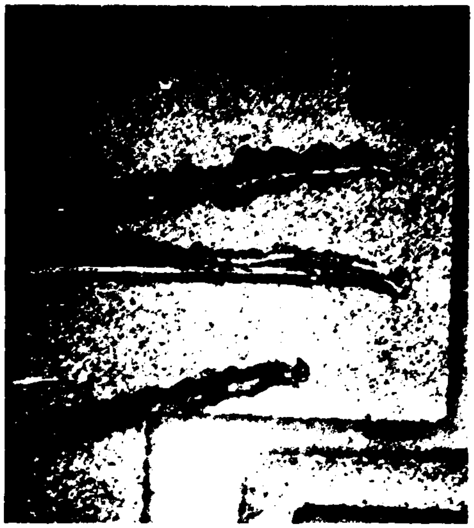


Figure 18. Englehard E-416-A intentionally fabricated with low adhesion.

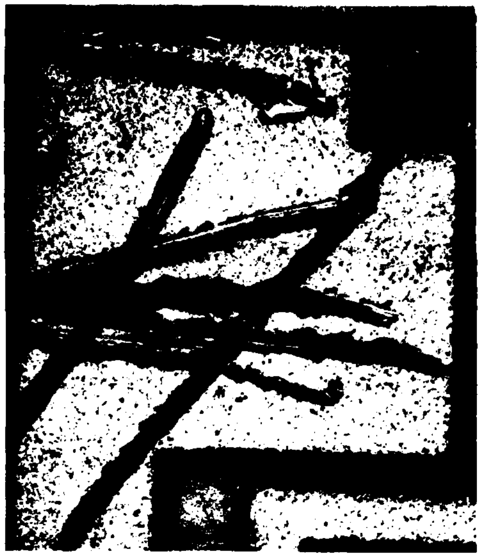


Figure 19. ESL 8831-A intentionally fabricated with low adhesion.

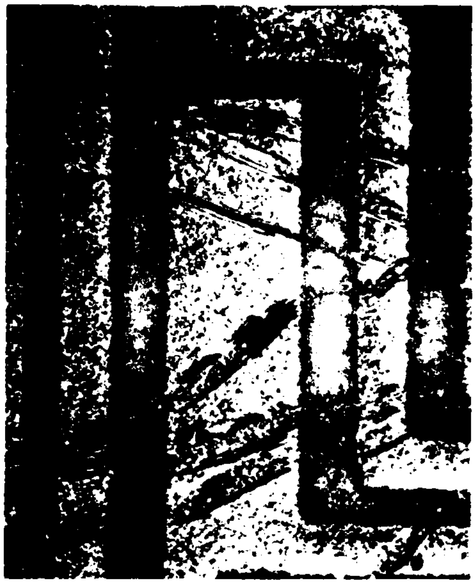


Figure 20. Engelhard E-416-A normal quality.

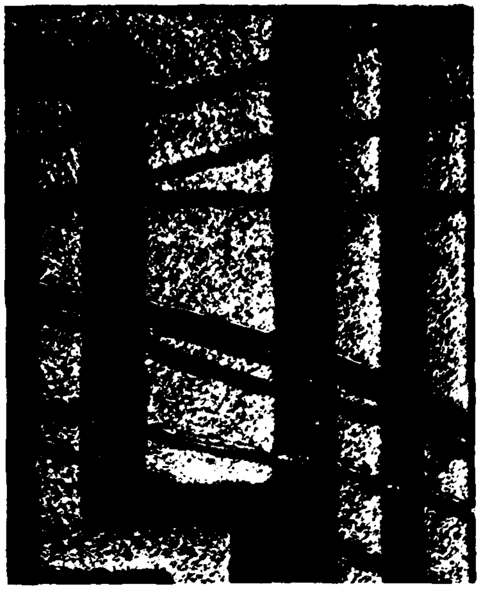


Figure 21. ESL 8831-A normal quality.

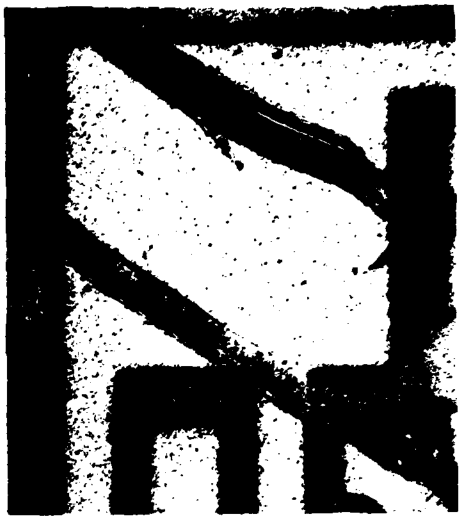


Figure 22. ESL 8831-A multilevel fabricated with low adhesion.

TABLE 17. ADHESION TEST SUMMARY

Thick Film	0.001 Au Loops	Lifted Metal (%)	$\overline{X}$ Lifted (gf)	Scratch Test Indicator
Engelhard E-416-A Fired Low, H266	117	18	18	Very flaky
ESL 8831-A Fired Low, H266	119	2	11	Slightly flaky
Engelhard E-416-A Normal Quality, H266	40	0	0	No flaking
ESL 8831-A Normal Quality, H266	39	0	0	No flaking
ESL 8831-A Fired Low Multilevel	174	6	23	No flaking

Testing of the thin-film used on this program showed no metal liftoffs when bonded with 0.002-inch Au wire and pulled destructively. Similarly, no adhesion problems were seen on die attach or wire bond areas in the hermetic packages purchased for the custom LSI integrated circuit.

For thin film substrates and package internal bonding locations, metal adhesion should be verified by bonding samples of the largest wire used in the device and by conducting a destructive wire bond pull test in accordance with Method 2011. Any evidence of metal liftoff from substrate or header is criterion for rejection. This testing may be done in conjunction with bondability testing.

3. ASSEMBLY CONTROLS

During the Evaluation Phase, use was made of assembly controls for substrate attachment, die attachment, and wire bonding. The intent was to determine if such controls should be applied as in-line processing requirements or as an out-of-line assessment. With an in-line test, the processing is interrupted while a destructive stress is applied to the entire lot. With an out-of-line test, samples are taken from the lot for destructive analysis while the lot processing continues at the risk of rejection on the basis of the analysis results. In either case, lot samples may be actual circuits or nonfunctional mechanical representative parts.

Figure 23 depicts a typical problem which can be attributed to insufficient adhesion between the thick-film metallization and the ceramic substrate. This example, taken from an internally funded study, shows a platinum-gold solder pad which has begun to lose adhesion after 50 temperature cycles in a ceramic chip carrier assembly test. This type of cracked appearance, which is actually thick-film liftoff, is also typical of that seen around some capacitor solder terminals following temperature cycling.

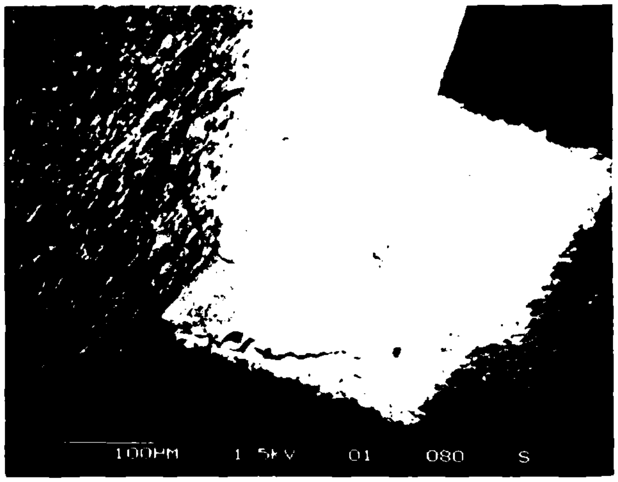


Figure 23. Loss of thick-film adhesion during temperature cycling.

Substrate attachment is normally tested by means of constant acceleration (centrifuge) on a lot-sample basis. When epoxy attachment is used, the entire lot is often attached and cured prior to testing on a 100 percent or sample basis, since the state of the epoxy and the cure cycle are important variables. However, this evaluation may be done in-line while control is exercised to ensure that the epoxy and cure cycle remain constant. Use of epoxy preforms allows an in-line evaluation by elimination of any pot-life variable. Chart recording on the cure oven provides a method of verifying that the sample is cured under the same conditions as the balance of the lot. Substrates used on this study utilized epoxy preforms and were found to be capable of withstanding 30 kg constant acceleration in an unsealed package. No substrate attachment failures were experienced in any phase of this program.

Chip capacitor and semiconductor attachment was by screen-printed gold-filled epoxy (one part mix) and was controlled by use of a die shear (push) test on a sample basis. This test was applied [illegible]ordance with the maximum shear level requirement of Method 2019.1 (u[illegible]o 5 kg force) with no failures to the criteria therein.

In both cases, testing was performed prior to temperature cycling during the Evaluation Phase. Data obtained from other programs during the course of this contract indicated the value of testing following temperature cycling for large area attachment. In at least two cases, failure during screening was attributed to improper attachment that could have been detected by temperature cycling followed by centrifuge or shear testing. For this reason, shear testing during the Validation Phase was performed on a nonfunctional sample following 10 temperature cycles, -55 to 125°C. This was done as an out-of-line process control, with further processing proceeding at risk pending the results. The production schedule for each lot was therefore indeterminable for approximately two days until the indication of proper attachment was received.

Wire bonding control was by 100-percent nondestructive bond pull testing in accordance with Method 2023. Although no major bonding problem was encountered on this program, events reported by other programs indicate that neither destructive nor nondestructive bond pull testing of the bonds as made can provide complete assurance of bond strength after temperature exposure. When a bimetallic system is used, additional intermetallic growth with subsequent processing and screening temperatures can reduce bond strength. In monometallic (Al) systems, the annealing of the wire can cause up to a 40 percent reduction in bond pull strength with later temperature exposure.

For each lot fabricated in the Evaluation Phase, a nonfunctional sample having approximately 30 wire loops of Al or Au wire was made as part of the lot. These units were subjected to 1 hour at 300°C and then destructively pulled to the postseal levels of Method 2011.2. Decrease of wire bond strength with temperature is a function of several variables that generally cannot be accurately predicted. Figure 24 shows the temperature response of aluminum wire bonds to gold-plated package posts as the power supply setting was varied on the ultrasonic bonder. In this sample the bonds having the highest initial strength suffered the greatest percentage of reduction in strength when subjected to 250°C for 2 hours.

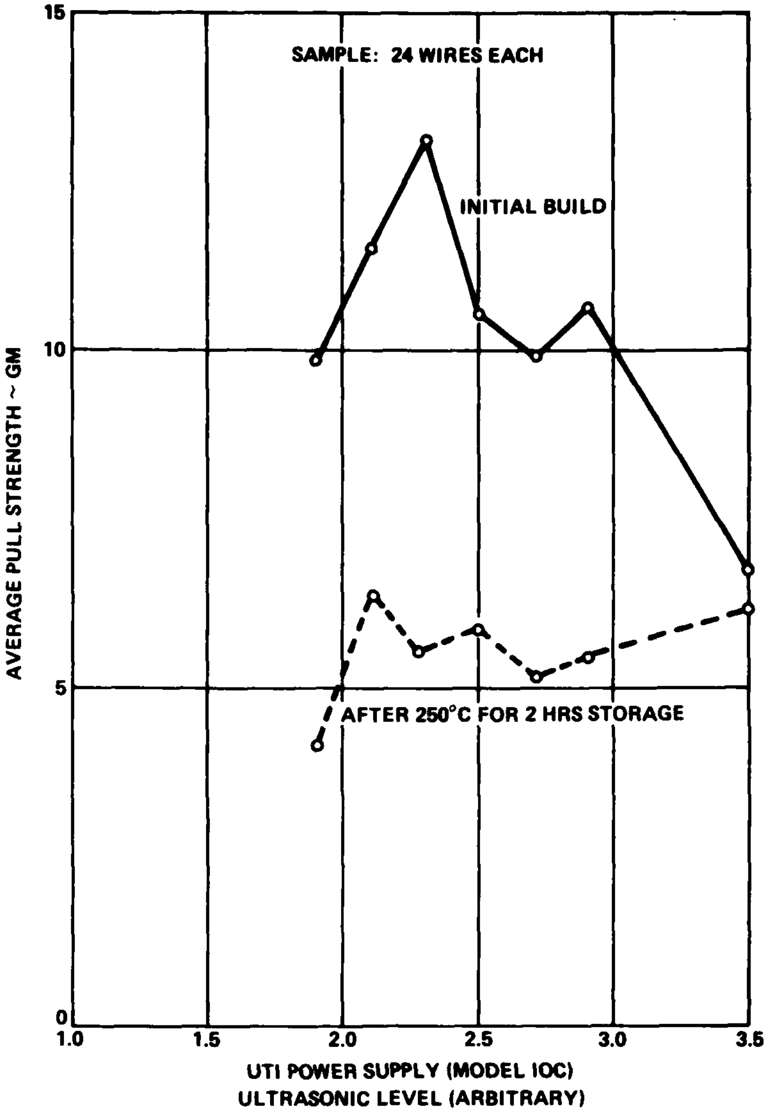


Figure 24. Variation in pull strength for Al wire on Au.

Figure 25 gives an indication of the rate of temperature effects on bond strength. These data exhibited an activation energy of 0.49 ± 0.1 eV for the degradation rate of bond pull strength based on the initial slopes. It should also be noted that for each temperature, there was an apparent lower limit to bond strength which was not reached in the case of those exposed at 150 and 200°C.

On the basis of such data, combined with a recent production lot that exhibited near-zero strength following temperature stress, the process control of subjecting a sample to destructive bond pull test following 2 hours at 250°C was instituted for the Verification Phase.

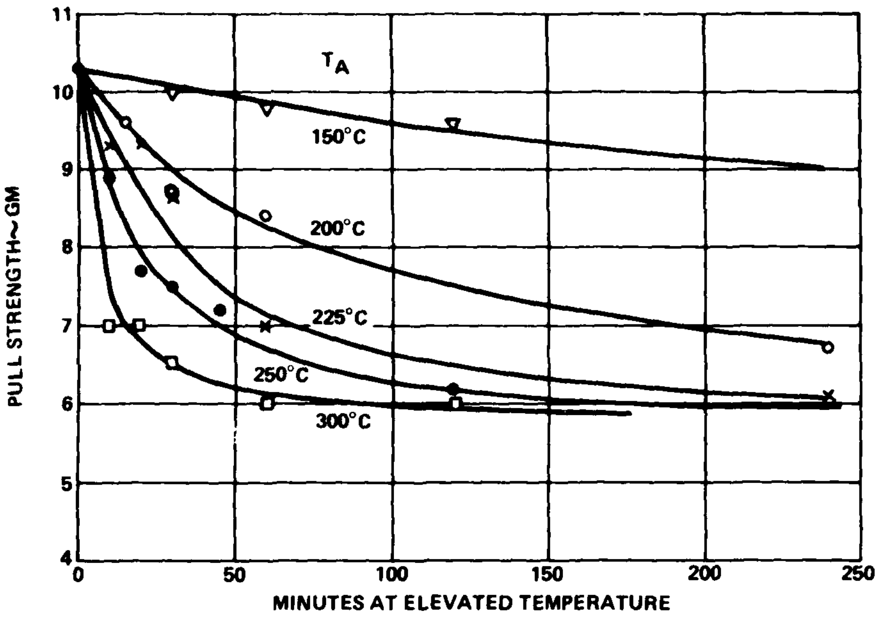


Figure 25. Al wire to Au bond strength temperature response.

For small lots, preseal electrical testing was done on a 100 percent basis rather than as a production control sample due to the equipment setup time in comparison to the time differential between testing a sample and the entire lot.

4. PRESCREEN MECHANICAL TESTS

An evaluation of mechanical shock and constant acceleration effects on hybrid devices was made using temporarily sealed platform packages and flatpaks. Sealing was with medium-strength room temperature curing epoxy which would degrade readily at 150°C to allow the packages to be opened and resealed at each level of the step stress testing.

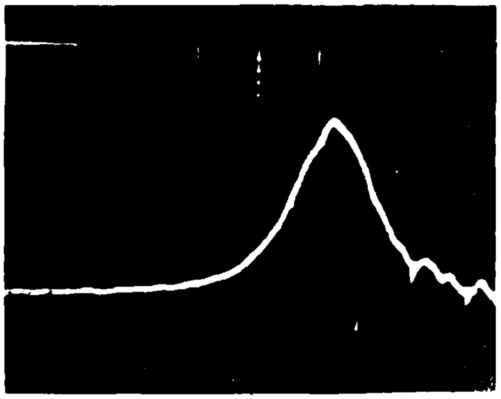
a. Mechanical Shock

Fixturing was done to perform mechanical shock on the 24-pin platform package containing the H266 hybrid. No electrical testing was to be done, so the test samples were fabricated with rejected semiconductor die and did not have trimmed resistors. Wire bonding was done using 0.001-inch gold wire. One subgroup contained only capacitors on the substrate.

Mechanical shock was delivered in the Y1 and X1 axis at each level using Conditions C through G of Method 2002.2. To avoid the cumulative effect of repetition of shock at lower levels, only one shock in each axis was used, and samples were alternated at lower condition levels. Both groups received the final 30 kg level. Group A was subjected to 3 kg and 10 kg shock pulses with no failures. Group B showed one wire bond failure at 5 kg and no defects at 20 kg. The lifted wire bond was defective due to overbonding at the post and had not been nondestructively pull tested or visually inspected. The 30 kg level was found to be excessive for both groups with 83 percent of the samples showing wire damage in the form of lifted bonds and bent wires. One capacitor was also dislodged in the subgroup which contained only chip capacitors without wire bonds.

Figures 26 through 32 are typical shock pulses applied as recorded on the package fixture. Figure 33 is typical of appearance following 30 kg pulse with two post bonds lifted and wires bent at the integrated circuit chip.

Figure 26. 3 kg, 0.3m SEC



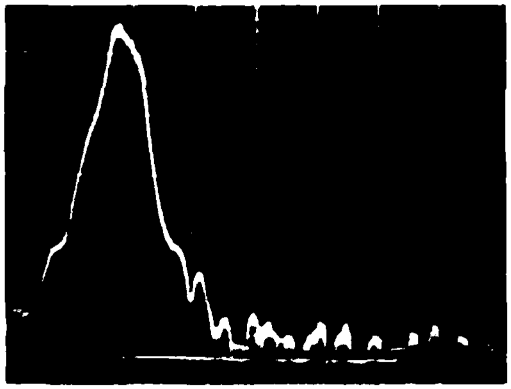
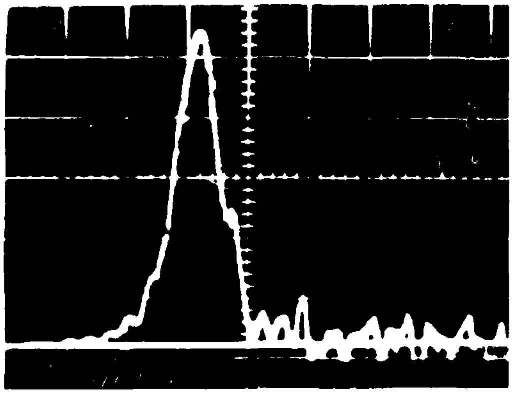


Figure 27. 5 kg, 0.3m SEC

Figure 28. 10 kg, 0.2m SEC



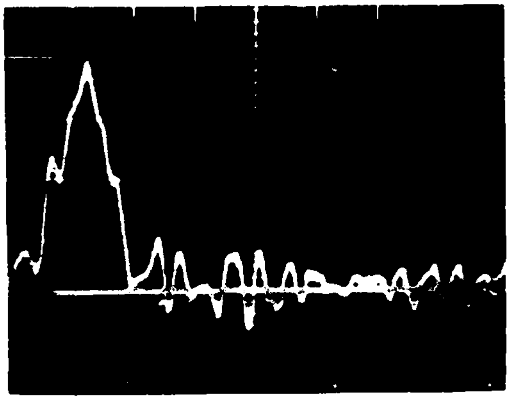


Figure 29. 20 kg, 0.2m SEC

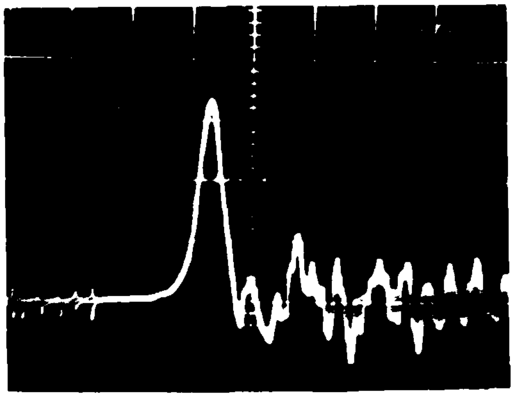


Figure 30. 30 kg, 0.1m SEC

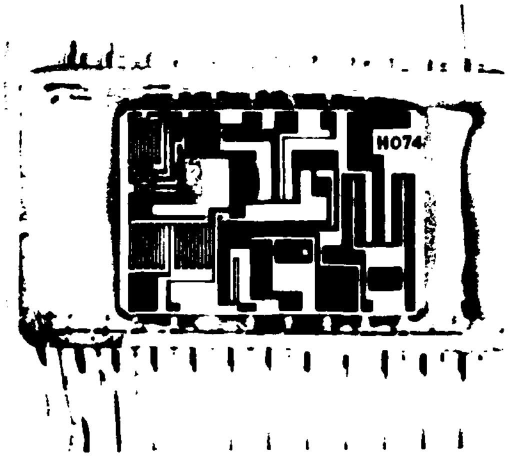


Figure 31. Chip capacitor separation at 30 kg constant acceleration.

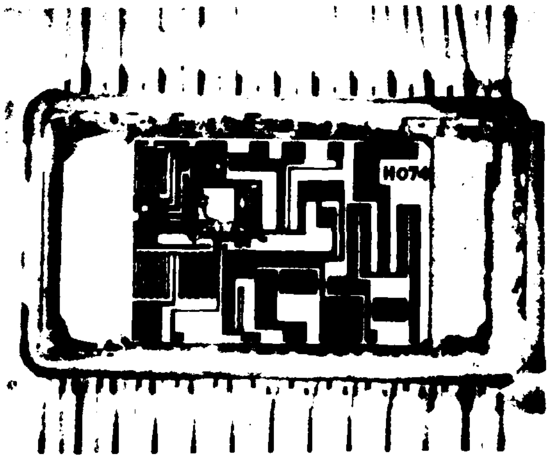
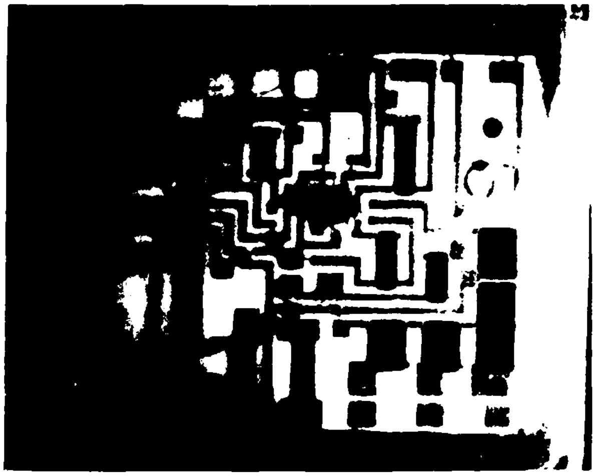


Figure 32. Ceramic chip capacitor fracture at 50 kg constant acceleration.

Figure 33. Typical 30 kg damage.



b. Constant Acceleration

The flatpaks subjected to constant acceleration, Method 2001.2, Conditions C, E, and F, contained a thin-film hybrid microcircuit with epoxy substrate and die attachment. Parts were divided into two groups with one exposed to 150°C bake for 24 hours prior to centrifuge testing. All units were stepped through all levels unless failure occured. As shown in Table 18, there is no important difference between the results for Groups A and B. Wire bonds had been measured on a sample basis prior to the test and showed an average destructive pull strength of 5.9 gram force for Group A following the 24-hour bake at 150°C, and 6.3 gram force for the units not receiving any temperature exposure. All units used Au wire bonds, so little degradation at 150°C was expected.

TABLE 18. CONSTANT ACCELERATION TEST RESULTS

Level (kg)	Condition	Group A (7 pieces)	Group B (15 pieces)
15	C	1 capacitor broken	1 capacitor broken
30	E	1 capacitor broken	6 capacitors broken or separated 2 with bent wires
50	F	3 capacitors broken Wire damage in same units only	2 capacitors broken 1 substrate broken Wire damage only on units having other damage

5. SCREENING

After sealing, each lot of LSI circuits and hybrids produced in the Evaluation Phase was split and subjected to two screening sequences. Parts in Sublot A were sent through normal screening shown in Table 19 as would be done in accordance with Test Methods 5004 or 5008 as applicable. The Sublot B units were screened to a short sequence which did not include temperature cycling or mechanical stress (Table 20). Hermeticity (seal) testing was done both before and after burn-in and initial electricals were included for both sublots to increase the completeness of the data.

TABLE 19. SUBLOT A NORMAL SCREENING SEQUENCE

Initial Electricals	Part Specification, 25°C
Stabilization Bake	Method 1008, Cond. C, 24 hrs.
Temperature Cycling	Method 1010, Cond. C
Constant Acceleration	Method 2001, Y1, Cond. E/B
Hermeticity	Method 1014, Cond. B & C
Interim Electricals	Part Specification
Burn-In	HTRB, Method 1015, 160 hrs.
Hermeticity	Method 1014, Cond. B & C
Final Electricals	Part Specification

TABLE 20. SUBLOT B SHORT SCREENING SEQUENCE

Initial Electricals	Part Specification, 25°C
Hermeticity	Method 1014, Fine and Gross, Cond. B and C
Burn-In	Method 1015, 160 hours
Hermeticity	Method 1014, Fine and Gross, Cond. B and C
Final Electricals	Part Specification, High and Low Temperature Limits

Table 21 summarizes the failures resulting from mechanical or environmental stress. Other electrical failures which occurred were found to be related to defects on the semiconductor die. Failure analysis reports which are included in Appendix B indicate a need for increased process controls.

TABLE 21. EVALUATION PHASE SCREENING RESULTS

Part Name (Hybrids)	Sublot A Qty	Sequence Failures	Sublot B Qty	Sequence Failures
H074	21	3 loose caps 1 wire bond	21	0
H266	23	0	22	0
72310026 (LSI CM001)	19	1 fine leak	19	0
Sidebraze-28	18	10 fine leaks 2 gross leaks	16	0
Sidebraze-40	16	3 centrifuge Excess camber	17	2 fine leaks
CERDIP-28	18	1 centrifuge 1 fine leak 3 gross leaks 2 wire bonds	15	5 fine leaks
CERDIP-40	12	4 gross leaks 2 wire bonds	14	2 fine leaks
Chip Carrier-28	12	0	14	0
Chip Carrier-40	15	0	16	0

6. FAILURE ANALYSIS

All devices which showed mechanical damage or electrical failures that could be indicative of mechanical damage were submitted to the Failure Analysis Laboratory. Typical failure analysis reports are included in Appendix B.

Failures observed in Sublot A, Table 21, showed several mechanical failures which could have been prevented by process controls. Three medium sized ceramic capacitor chips detached during centrifuge testing at 10,000g. These were attached with conductive epoxy with an expected minimum strength of 1500 psi in tensile. Each capacitor had a mass of 0.07 gram and an attachment area of approximately 4×10^{-3} square inch. At 10,000g acceleration the force on the attachment interfaces was approximately 400 psi, well below the expected strength distribution.

Since the entire lot was fabricated with the same epoxy and cured at the same time, the three failures may indicate a general weakness in the lot such that even those parts passing screening are suspected of being marginal. This supports the need for a process control capable of verifying that the epoxy has at least a minimal strength after exposure to temperature equivalent to complete device processing and screening.

The bonding wires which showed failure at low mechanical stress levels were also suspected of being representative of a general bonding problem. Failure analysis showed an exposure to excessive sealing temperature on the glass frit (CERDIP) packages resulted in intermetallic growth and weakened bonds. Other package types showed bond failures were due to misplaced bonds, overbonds, and damage prior to seal. In the former case, a process control would have been effective only if it included the equivalent to the sealing and subsequent screening temperatures. In the latter case, some of the substandard bonds could have been detected in pre-seal visual inspection while others were random defects not likely to be detected through sampling.

Leak failures were detected in both sublots and were attributed to an improper sealing profile for the CERDIP packages and weak solder seals on the side braze packages. The full sequence which included temperature cycling detected slightly more fine leaks (not thought significant) and all of the gross leaks observed. Since the CERDIP packages were sealed with a non-optimized profile, activation of gross leak failures by temperature cycling is to be expected.

Four package failures occurred during centrifuge on parts having excessive camber. These could have been prevented by fixturing or by tightening part specifications. Since the characteristic leading to failure is not important to part application, precautions should be taken to insure fixturing which will distribute the load over the package surface.

7. EVALUATION PHASE FINDINGS

Several areas for recommendations were established on the basis of the Evaluation Phase. These were included as supporting arguments in the Verification Plan (Appendix A). A summary of these recommendations follows.

1 Perform temperature cycling as a precondition to testing for die attach and substrate attach.

2 Use temperature cycling in conjunction with leak testing or lid torque testing to control the sealing process.

3 If the above process controls are utilized, investigate dropping temperature cycling from the screening sequence.

4 Use thermal shock for package qualification or material acceptance but not as a screen.

5 Retain constant acceleration in the screening sequence due to low cost/benefit ratio. Except when fixturing is required for a special package, the cost is low.

6 Do not use mechanical shock as a bonding screen.

7 Retain solderability requirements but consider expanding for new package styles such as chip carriers.

8 Consider combining moisture resistance testing with ionic susceptibility testing now done by salt atmosphere.

SECTION V

VERIFICATION PHASE

The validity of the recommendations resulting from the Evaluation Phase were tested in the Verification Phase, which involved building products similar to those tested earlier for which additional process controls had been instituted. As shown in Appendix A, two screening sequences were proposed to determine if the process controls as instituted were sufficient to obviate the need for mechanical screening tests. An additional consideration was predicated on proposed revisions to Method 5008 which would require 100-percent screening of passive chips; see chip capacitor screening discussion, Section III, subsection 3. No preseal testing, except for nondestructive bond pull on hybrids, of actual test samples was done in an effort to minimize the number of test variables.

1. VERIFICATION TEST RESULTS

Table 22 summarizes the results of testing in accordance with the normal 5008 sequence (Sublot A) and a modified sequence defined in the Verification Plan (Sublot B). As during the Evaluation Phase, the analysis was confined to failures which were mechanical or which had electrical characteristics that indicated a mechanical or environmental cause of failure. A higher incidence of electrical failures was attributed to the lack of electrical testing prior to seal on the hybrid devices.

TABLE 22. VERIFICATION PHASE SCREENING RESULTS

Part Name (Hybrids)	Sublot A Sequence Qty	Sublot A Sequence Failures	Sublot B Sequence Qty	Sublot B Sequence Failures
H074	10	0	10	0
H266	10	0	10	0
72310026 (LSI CM001)	10	2 fine leaks	10	3 fine leaks
Sidebraze-40	15	0	15	1 gross leak
CERDIP-28	27	6 fine leaks	27	10 fine leaks
CERDIP-40	23	0 see failure analyses	22	1 fine leak 1 gross leak 2 wires sagging
Chip carrier-28	14	0	14	0
Chip carrier-40	28	1 gross leak (not detected)	25	1 gross leak

It should be noted that drop shock at 3 kg did not appear to directly replace the constant acceleration used in the Evaluation Phase. During the verification phase there were only two mechanical failures not associated with package hermeticity. The types of failures produced by shock were also different in that constant acceleration showed removal of capacitors and loose wire bonds, whereas drop shock resulted in movement in the wire span in the form of sagging or lateral shifting of the loop. The absence of chip and wire bond removal in drop shock was attributed to the additional process controls implemented on Sublot B.

The test sequence did not appear to affect the test results since the distribution of rejects was approximately the same, with the exception of the two drop shock failures which had been through a shorter sequence at the time of failure; i.e., burn-in was done following mechanical testing on that sublot.

Review of the failure analysis results indicates that neither sequence utilized in the verification phase was capable of detecting the poor lead dress which was evident in the 40-pin CERDIP packages. It is theorized that improper fixturing put stress on the lead frame during sealing which caused the lead frame pins to shift upward and remove the small loops in the bonding wires. Completely taut wire such as observed cannot be expected to exhibit long life in field operation and would probably fail because of temperature cycling.

2. VERIFICATION FAILURE ANALYSIS

Devices which were intentionally fabricated with reduced controls and non-standard assembly techniques tended to fail due to seal leakage or moisture within the package. Many of the leak failures were attributed to blow holes in the sealing material caused by the use of nonqualified die attachment techniques. Epoxy used for die attachment was not the type normally used in packages which will see a high temperature package sealing method. The resultant outgassing during the seal caused high internal pressure and produced leakage paths on both glass frit seals and solder seals.

Also attributed to the incomplete control of materials and the sealing profile are the moisture-related electrical failures in the CERDIP packages. Normal precautions such as package bakeout and epoxy postcure vacuum bakeout were not applied, with a resultant high moisture level within the sealed package that was sufficient to cause some failures even during the burn-in and short electrical tests.

Figures 34 through 43 are typical of the failure analysis results observed.

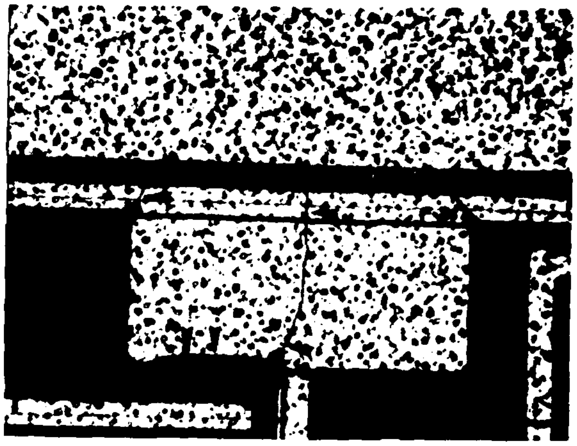


Figure 34. Aluminum corrosion, 40-pin CERDIP.

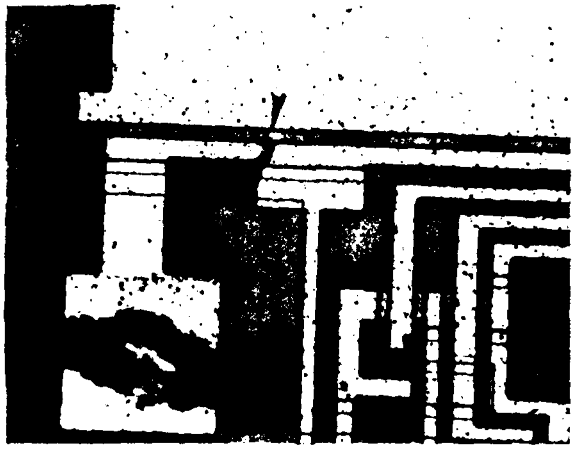


Figure 35. Open circuit, 40-pin CERDIP.

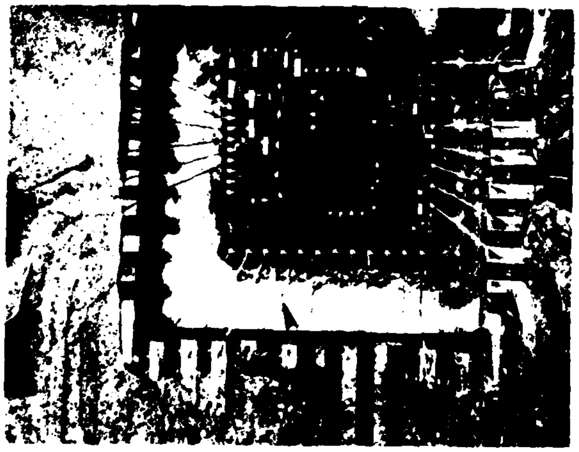


Figure 36. Displaced wire loop shorted to adjacent wire, 40-pin CERDIP.

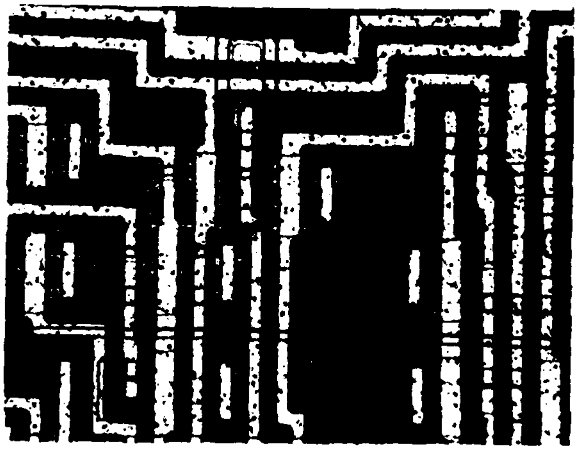


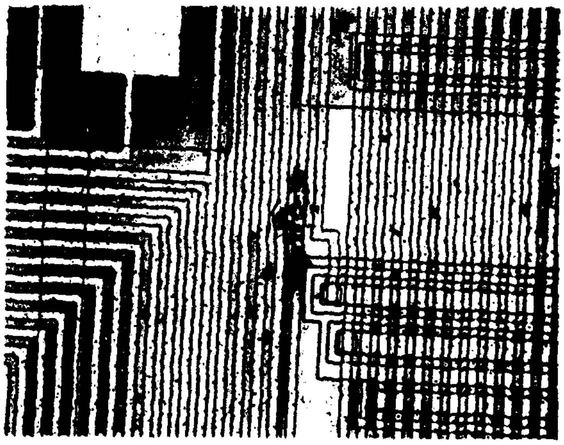
Figure 37. Diffusion anomalies, electrical failure, 28-pin CERDIP.

Figure 38. Taut bond wires not detected, 40-pin CERDIP.

Figure 39. Solid seal blow hole, chip carrier SN 149.

Figure 40. Leakage path, 40-pin Sidebraze, SN 124.

Figure 41. Metallization damage, chip carrier SN 149.



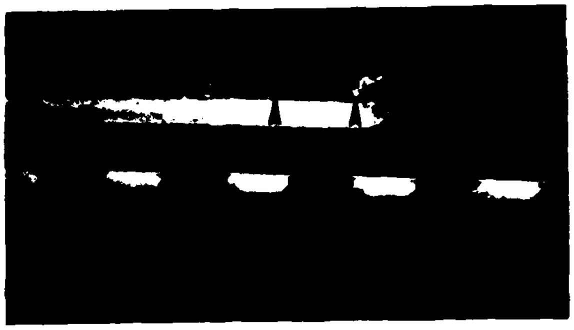


Figure 42. Solderseal leak, 40-pin Sidebraze, SN 124.

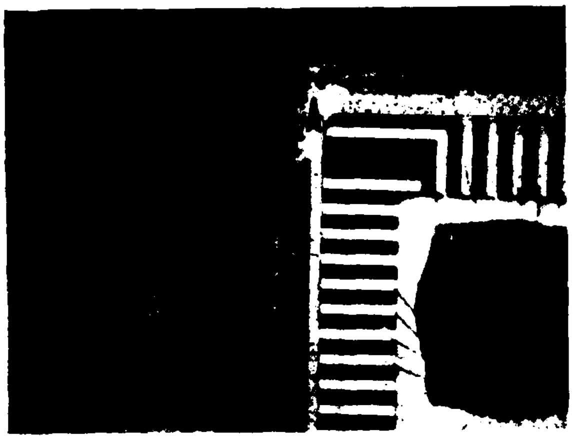


Figure 43. Leakage path, 40-pin Sidebraze, SN 124.

SECTION VI

CONCLUSIONS AND RECOMMENDATIONS

The control of quality and reliability related variables for LSI devices fabricated in small lots is dependent on variations in materials and processes and the resultant interactions. Qualification of packages and materials does not ensure the quality of similar constituents used in future products. An evaluation of incoming material in conjunction with process controls can be used to detect problems prior to incurring assembly and test costs.

Specified considerations to provide increased levels of product assurance are listed below:

1 Packages could be standardized and qualified by the package manufacturer. This would allow the user to concentrate at incoming testing on such items as plating quality, sealing surfaces, and wire bonding posts, which are expected to vary considerably.

Tests which could be performed by the package manufacturer to qualify a package design include:

a. Verification of physical dimensions
b. Solderability
c. Seal (unlidded)
d. Metal package isolation
e. Lead integrity following temperature conditioning
f. Moisture resistance with salt contamination
g. Metal package isolation when applicable.

Of these, only the addition of salt contamination to the moisture resistance test would differ from the existing MIL-STD-883 methods. This variation would provide for a preconditioning of packages by dipping in a 0.1 percent salt (sodium chloride) solution and air drying prior to commencing the moisture resistance test. Package users should submit package samples to at least a plating verification including a high temperature exposure (350°C for 5 minutes) and a sealing verification using normal leak tests on sealed packages.

PRECEDING PAGE BLANK-NOT FILMED

2 Hybrid substrate thick-film adhesion testing is subjective but essential for applications such as solder attachment of components where high adhesion strength at the thick-film solder pads is required.

If the device is to use solder attachment of components, a sample of substrates should be subjected to the following:

a. Solder pull wires to bonding pads approximately 100 mils square
b. Temperature cycle Method 1010, Condition B, 50 cycles min.
c. Perform peel test by lifting wire end vertically and observing at least 800 psi adhesion.

If the device will use polymer attachment of components, the pull wires should be so attached and cured. Temperature exposure may be 24 hours at 125°C followed by peel testing to the 800 psi adhesion criteria.

Thin film and bonding post plating should be tested by destructive pull testing of wire bonds and observing no lifted metallization.

3 Bondability of hybrid thick - and thin - film metallization can be determined with sample bond and pull tests. Poor bondability can be compensated for by adjustment of the bonding schedule, a more significant variable.

Bondability tests should be performed on sample substrates prior to commitment to assembly.

4 Temperature cycling is the primary activator for many failure mechanisms associated with LSI integrated circuits and hybrids. This is due to the large dimensions which allow high stress due to the mismatch of the thermal coefficient of expansion.

5 High temperature is an efficient activator of plating and bonding defects.

An inexpensive test of gold plated packages can be done by subjecting a sample to 350°C for 5 minutes and examining to visual criteria of Method 2009.

6 Drop shock produces different results than does constant acceleration when applied to wire bonds. Drop shock is not an acceptable screening mechanism since the passing parts may be degraded.

7 External visual inspection criteria should be clarified based on the package characteristics.

Visual inspection criteria of Method 2009 should differentiate between glass frit sealed, multilayer ceramic, and glass to metal lead seal packages.

8 The existing Methods 5004, 5005, and 5008 which provide for qualification and screening are not directly applicable for LSI microcircuits manufactured in small lots.

A new test method should be formulated for inclusion in MIL-STD-883 to provide quality assurance procedures for LSI microcircuits in small lots. The method should emphasize process controls as discussed herein to avoid the low confidence associated with previous qualifications and the high cost and schedule implications of poor yields at screening.

9 Constant acceleration testing activates failure mechanisms which could be eliminated by process controls. However, due to the low cost, this method is cost-effective as a screen and as a detector of process control escapes.

An analysis of any failures resulting from constant acceleration at low levels should be made to determine the severity of the problem throughout the lot. When Method 2001 is specified at Condition B, a PDA (percent defective allowable) of 10 is reasonable since a specific out of control condition is indicated.

10 Die shear testing as presently specified does not adequately evaluate attachment of large semiconductor die or noneutectic attachment.

An alternative method which provides for die liftoff testing using a quick curing adhesive and a vertical pull tool should be included in MIL-STD-883.

11 Screening of passive chip components for hybrids is not cost effective. Both semiconductor and passive chip components should be tested on a sampling plan using an LTPD=10. For critical applications the tests should include both high and low temperature parameters.

12 Salt atmosphere testing should be limited to those parts which will be exposed to corrosive atmospheres. Other packages should be qualified by the manufacturer by preconditioning in a 0.1 percent sodium chloride solution prior to performing moisture resistance testing.

13 Solderability is sufficiently tested for leaded devices by the present method. However, a test method should be defined to evaluate leadless ceramic chip carriers. Acceptable packages should be able to withstand 3 dips in accordance with Method 2003.2 paragraph 3.4 except at 230°C. No more than 15 percent of any solder attachment pad should show evidence of leaching or dewetting.

APPENDIX A

VERIFICATION PLAN

PRECEDING PAGE BLANK-NOT FILMED

VERIFICATION PLAN
QUALITY ASSURANCE PROCEDURES
FOR LSI

July 15, 1980

CDRL A002

CONTRACT F30602-79-C-0071
ROME AIR DEVELOPMENT CENTER
GRIFFISS AFB, N.Y. 13441

Prepared by: Lee Mirth
Lee Mirth
Task Leader

Approved by:
Rolf Linden
Mgr./Hybrid Dev
Eng'r.

Martin Marietta Aerospace

Orlando, Fl 32855

1.0 Introduction

The verification phase will be conducted in accordance with the work statement, paragraph 4.4 and the Martin Marietta proposal OR 15,166P. Sample sizes will be as stated in Martin Marietta letter to John P. Farrell dated 7 April 1980 and agreed to in Rome Air Development Center letter dated 7 May 1980.

2.0 Sample Description

50 each: CM001 Custom LSI in the following packages:

- CERDIP, 28 and 40 leads
- Hermetic Chip Carrier, 28 and 40 pin
- Multilayer Side Braze, 28 and 40 lead

20 each:
- H074 Thin Film Hybrid in a 24 lead flat package
- H266 Thick Film Hybrid in a 24 lead platform package
- 72310026 Multilevel Thick Film Hybrid in a 44 lead platform package

Test samples will be fabricated in a single lot with one half of the devices designated for normal screening and the other half designated for the alternate techniques described herein.

3.0 Evaluation Phase Summary

Testing conducted during the evaluation phase has been supplemented by internal studies and problem investigations from production units. Several areas for improved or optional test techniques are indicated by the data and are candidates for verification. Significant areas which were investigated during the evaluation phase include the package damage criteria in support of Method 2009. The recommended revisions are based on adequate data to obviate the verification phase for chip-out criteria.

3.1 Temperature Cycling Results

No failures were attributed to temperature cycling on units produced under this contract. However, other custom LSI devices produced during the contract term showed temperature cycling damage during screening on particular units due to processing anomalies. Since temperature cycling exercises constituent interfaces through coefficient of expansion inequalities and dimensional processing variations, its use as a screen of the completed product appears not to be cost-effective. In particular, the last processing step which results in an interface of dissimilar materials is the optimum point for temperature cycling evaluation. This, of course, varies with the type of constituent attachment, circuit intraconnection, and packaging system used.

Where the susceptibility to temperature cycling induced failure is dependent on normal processing conditions rather than localized anomalies, a lot sample may be sufficient. An example of this would be the package sealing process for CERDIP packages wherein an improper temperature profile would affect the entire lot.

Temperature Cycling Recommendations

Conduct temperature cycling following die attach as a precondition for die shear testing and, where applicable, substrate attach testing. Utilize temperature cycling in conjunction with leak testing and lid torque testing to control seal process parameters. Eliminate temperature cycling from the screening sequence on the finished product.

3.2 Thermal Shock Results

Package evaluation and qualification utilized thermal shock with limited success. Some faulty glass-to-metal seals have been activated to failure by this method on other Martin Marietta programs but it is felt to be too severe for a screening test. The method has also been used to evaluate substrate attach materials and solder joints. However, lots which were unable to withstand ten thermal shocks were found capable of withstanding 100 temperature cycles to Method 1010 Condition B.

Thermal Shock Recommendations

Do not impose this method as a screen. Use for package qualification and lot acceptance or material evaluation.

3.3 Constant Acceleration Results

Failures were observed on the custom hybrid device, H074, following Method 2001, Condition B. Three failures were attributed to chip capacitor epoxy attachment. One was found to be an Al wirebond separation at the chip. Since this wire had successfully undergone non-destructive wire pull testing, failure at 10 kg acceleration was unexpected.

Gold bond wire failures were observed on LSI CERDIP packages after Condition E testing. These were due to intermetallic formations on the posts which were designed for Al wirebonding. With the exception of the Al wirebond failure mentioned previously, all failures occurred at sites where the Martin Marietta design guidelines had been violated; chip capacitors normally receive epoxy overbonding for mechanical strength and the CERDIP package is designated for an all Al system. The Al wirebond which failed could have been found defective at visual inspection since less than 50% of the bond area was on the bonding pad.

Martin Marietta's experience on various production programs has shown that failures during constant acceleration are indicative of improper material design or insufficient process control. Very few constant acceleration failures occur on mature, normally processed devices. Several side brazed packages cracked during constant acceleration. This was attributed to excessive camber which caused unequal stress on the packages.

Constant Acceleration Recommendations

Consider retaining constant acceleration in the screening sequence due to the low cost and occasional major benefit. Utilize constant acceleration after temperature cycling for process control of substrate and chip attachment prior to additional labor investment in the devices. Where packages may be mounted so as to bear on the package surface, the camber should be controlled by lot acceptance.

3.4 Mechanical Shock Results

Samples were subjected to drop shock testing using the AVCO amplifier to achieve levels up to 30 kG. Two groups were step stressed at alternate levels corresponding to Method 2002 test Conditions C through G. At each level, shocks were applied in the Y1, X1, and Z1 axis. Typical pulse recordings are shown in Figures 1 through 5.

The package chosen for this test was a 24 pin platform which is a consistently reliable configuration. This package allowed temporary cover attachment with epoxy such that units could be delidded and visually inspected after each shock series. Test samples utilized non-conductive epoxy substrate attachment, two types of thick film metallization, chip capacitors, a variety of semiconductors, and both Al and Au wirebonds. Separation of wirebonds and capacitors was anticipated at higher shock levels.

Both the 30 kG level, results showed one failure due to a lifted Al wirebond and five failures due to handling. The lifted wirebond occurred at 5 kG and was attributed to overbonding. All units had passed non-destructive bond pull testing in accordance with Method 2023.

Several failures occurred at 30 kG as expected. All six units having Au wires showed bent wires and lifted bonds indicating the non-destructive test limit had been exceeded. One of the six units with Al wires showed bond failures attributed to mishandling. Six units containing only substrates and chip capacitors experienced a single capacitor separation at 30 kG. Capacitors were not overbonded in contrast to normal Martin Marietta guidelines.

Mechanical Shock Recommendations

Handling difficulties make mechanical shock of unsealed packages difficult to implement without special fixturing, shock levels necessary to find marginal bonds appear excessive (30 kG). Therefore, mechanical shock is not recommended as a bonding screen.

Substrate and chip attach could be evaluated by mechanical shock but can be more easily evaluated by die and substrate shear tests or constant acceleration tests.

Perform temperature cycling and drop shock on 50% of the alternate screen group following all other environmental screens. Utilize a flatwise drop, Y1 axis, 16 ft/sec.

3.5 Solderability Results

All packages passed solderability testing. The present method appears to be adequate for the packages under consideration.

Solderability Recommendations

Retain solderability requirements in Method 5005 and 5008. Expansion of solderability tests for applications such as chip carriers on boards using various material and metallizations should be a separate study.

3.6 Moisture Resistance Results

Testing on a variety of packages was ineffective in detecting exposed basis material and moisture penetration. Analytical examination of the existing method indicates that it is well founded with the exception of an ability to detect moisture ingress to the package interior and the ability to evaluate the packages' susceptibility to ionic contamination. Exposure of the packages to low levels of contamination prior to the moisture resistance cycle would be more indicative of the part's ability to withstand conditions of board mount and field use. This would also obviate the salt atmosphere test.

Moisture Resistance Recommendations

Retain as a requirement for package evaluation with the addition of a brief immersion in a normal salt water solution prior to the present test. Omit the salt atmosphere test requirement from package evaluation.

4.0 Testing Sequence

All recommendations will be verified by submitting samples to the tests required by Methods 5005 and 5008 with the modifications outlined in the previous sections. For the hybrid devices, substrates previously characterized will be used. Fabrication of test samples will be by normal custom LSI and custom hybrid production techniques.

4.1 Modified Testing

The remaining 50% of the test samples will be subjected to modified process controls and a modified screening sequence as outlined in Tables I, II and III.

TABLE I Additional Process Controls

Step	Method	Sample
Substrate Attach	Temperature Cycle 1010,C Constant Acceleration 2001, B, Y1	2
Chip Attach	Temperature Cycle 1010, C Die Shear Strength 2019	2
Wire Bonding	High Temperature 1008, F, 5 min. Bond Strength 2011	2
Lid Torque (CERDIP only)	Temperature Cycle 1010 C Lid Torque, Level TBD	2

TABLE II CHIP TESTING

Active Chips	Method
LSI Wafer Inspection	Martin Drawing
Internal Visual	2010, 2072, 2073
Temperature Cycling	1010, Cond C
Final Electricals	5008, Group A
Capacitors	
Thermal Shock	MIL-C-55681B, Para. 4.7.11
Voltage Conditioning	MIL-C-55681B, Para. 4.7.3
Electrical Parameters	Dielectric Withstanding Voltage Insulation Resistance Capacitance Dissipation Factor

TABLE III MODIFIED SCREENING SEQUENCE

Screen	Method
Internal Visual	2010, B/2017
Initial Electricals	Device Spec., 25°C
Burn-in	1015, 125°C, 160 Hrs.
Hermeticity	1014
*Interim Electricals	Device Spec. 25°C
*Temperature Cycling	1010, C
*Drop Shock	Equivalent to 3kG - Special Fixture
Final Electricals	Device Spec., 25°C

*Perform Temperature Cycling, Drop Shock and Interim Electricals prior to Burn-in on 50% of samples.

Quality Conformance Sample Selection

5005, Group B, Subgroup 6 for LSI and 5008, Group C, Subgroup I for hybrids.

APPENDIX B

EVALUATION PHASE FAILURE ANALYSIS REPORTS

MARTIN MARIETTA

PHYSICS OF FAILURE LABORATORY
ANALYSIS REPORT

THIS SHORT FORM REPORT SUMMARIZES THE (1) HISTORY, (2) ANALYSIS PROCEDURE, (3) CONCLUSION (CAUSE), (4) RECOMMENDATIONS.

HISTORY:

THESE TWO DEVICES WERE SUBMITTED FOR DECAPPING AND INTERNAL VISUAL EXAMINATION AFTER HAVING BEEN SUBJECTED TO SCREENING AND QUALIFICATION TESTS.

GPA

EXAMINATION:

VISUAL EXAMINATION OF THE DIE CAVITY WAS PERFORMED IN ACCORDANCE WITH MIL-STD 883 METHODS. USING LIGHT OPTICAL MICROSCOPES HAVING MAGNIFICATIONS FROM 10X TO 250X AND BOTH BRIGHT FIELD AND DARK FIELD ILLUMINATION.

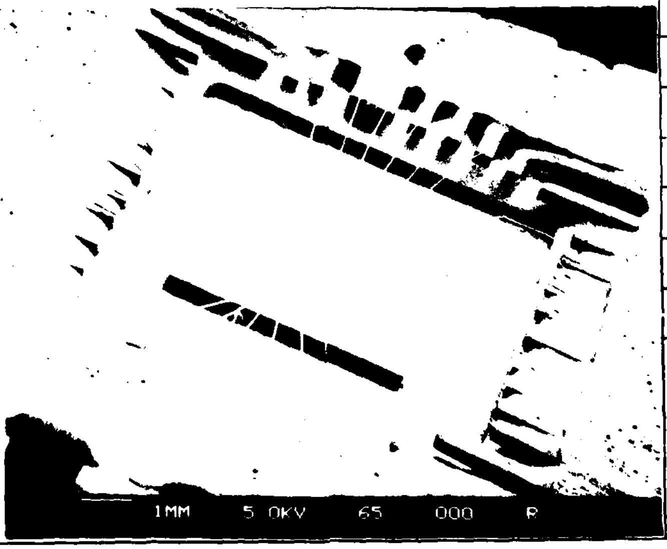
RESULTS:

THE DIE CAVITY WAS CLEAN. EACH DEVICE HAD A HALF DOZEN OF ITS GOLD BOND WIRES SEPARATE FROM THE LEAD POST BOND. THESE WERE LIFTED AND BENT SO AS TO INDICATE IMPACT WITH THE INNER SURFACE OF THE LID. (SHOCK OR ACCELERATION FAILURE.) INTERMETALLIC FORMATIONS WERE EVIDENT ON ALL 29 BOND PADS AND MOST OF THE LEAD POST BONDS. THE LEAD FRAME IN ADDITION TO BEING ALUMINUM PLATED HAD POOR LEAD POST ALIGNMENT WITHIN THE CAVITY. SOME TRANSLUSCENT GRAY DROPLETS WERE FOUND ON THE DIE SURFACES IN EACH DEVICE. THESE APPEARED TO BE GLASS FRIT WHICH WERE WETTED TO THE PASSIVATION LAYER.

NOTE: SEE APPENDED PAGES OF PHOTOS FOR BOND DETAILS.

PHOTO 1 10X

OVERALL VIEW



PAGE 1 OF 1

ANALYSIS NO.
LAR# 00123

PROJECT
QA-LSI

SOURCE DOC. NO.
NA

PART NAME
INTEGRATED CIRCUITS

MODEL NO. CERDIP-40
S/N - DATE CODE 65167- 8011

DRAWING NO.
NA

SUPPLIER
MARTIN MARIETTA MEC

ORIGIN OF FAILURE
NA

FAILURE CODE
☐☐ ☐☐ ☐☐

REMARKS:

VERBAL REPORT
TO: L. MIRTH x 3261

DATE: APRIL 30, 1980

CORRECTIVE ACTION RECOMMENDED:

SUPPLIER ______

MFG. ______

TEST ______

ENG. ______

OTHER ______

DATE COMPLETE:
MAY 5, 1980

ANALYSIS ENGR.
E. L. Zigler x3046

COMP. DES. ENGR.
Lee Mirth

APPROVALS:

SAMPLE DISPOSITION:
RETAINED ☐ RETURNED ☒

Form D-1672
Mar70

MARTIN MARIETTA

PHYSICS OF FAILURE LABORATORY ANALYSIS REPORT

THIS SHORT FORM REPORT SUMMARIZES THE (1) HISTORY, (2) ANALYSIS PROCEDURE (3) CONCLUSION (CAUSE) (4) RECOMMENDATIONS.

HISTORY:

THESE THREE DEVICES WERE SUBMITTED FOR DECAPPING AND INTERNAL VISUAL EXAMINATION AFTER HAVING BEEN SUBJECTED TO SCREENING AND QUALIFICATION TESTS.

EXAMINATION:

VISUAL EXAMINATION OF THE DIE CAVITY WAS PERFORMED IN ACCORDANCE WITH MIL-STD 883 METHODS USING LIGHT OPTICAL MICROSCOPES AT MAGNIFICATIONS FROM 10X TO 250X AND BOTH BRIGHT FIELD AND DARK FIELD ILLUMINATION.

RESULTS:

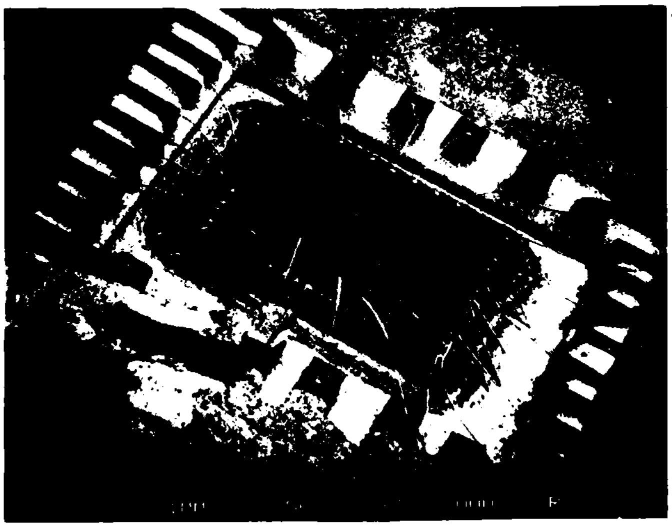
SERIAL NUMBER 16 HAD ALUMINUM ULTRASONIC WIRE BONDING. THE WIRES WERE ALL IN GOOD CONDITION WHEN THE GLASS FRIT PACKAGE WAS DECAPPED. (GP B)

SERIAL NUMBERS 36 AND 37 CONTAINED ALL GOLD ULTRASONIC WIRE BONDING. SN 36 HAD 4 WIRES SEPARATED FROM THE LEAD POSTS AND PULLED UP AGAINST THE LID. SN 37 HAD 8 WIRES LIFTED IN THE SAME MANNER AND TWO WIRES WHICH HAD SEPARATED AT THE BOND PAD AS WELL AS AT THE LEAD POST. INTERMETALLIC FORMATIONS WERE OBVIOUS AT MOST BOND LOCATIONS. (GP. A .)

NOTE: SEE APPENDED PAGES OF PHOTOS FOR BONDING DETAILS.

PHOTO 1 10X

OVERALL VIEW



PAGE 1 OF 1

ANALYSIS NO: LAR# 00124

PROJECT: QA-LSI

SOURCE DOC NO: NA

PART NAME: INTEGRATED CIRCUITS

MODEL NO: CERDIP-28 S N: 16,36,37 - DATE CODE: 8011

DRAWING NO: NA

SUPPLIER: MARTIN MARIETTA MEC

ORIGIN OF FAILURE: NA

FAILURE CODE: ☐☐ ☐☐ ☐☐

REMARKS:

VERBAL REPORT TO: L. MIRTH X3261

DATE: APRIL 30, 1980

CORRECTIVE ACTION RECOMMENDED:

SUPPLIER ______

MFG ______

TEST ______

ENG ______

OTHER ______

DATE COMPLETE: MAY 5, 1980

ANALYSIS ENGR: E. L. Zigler X3046

COMP. DES. ENGR: Lee Mirth

APPROVALS:

SAMPLE DISPOSITION:

RETAINED ☐ RETURNED ☒

Form D-1872 Mar 70

APPENDIX TO: LAR # 00124 AND 00123 PAGE 1 OF 2

PHOTO 1 SN 037 200X

THIS IS A VISIBLE LIGHT MICROPHOTOGRAPH SHOWING THE INTERMETALLIC FORMATIONS FOUND IN THE GLASS FRIT SEALED CERDIP PACKAGES.

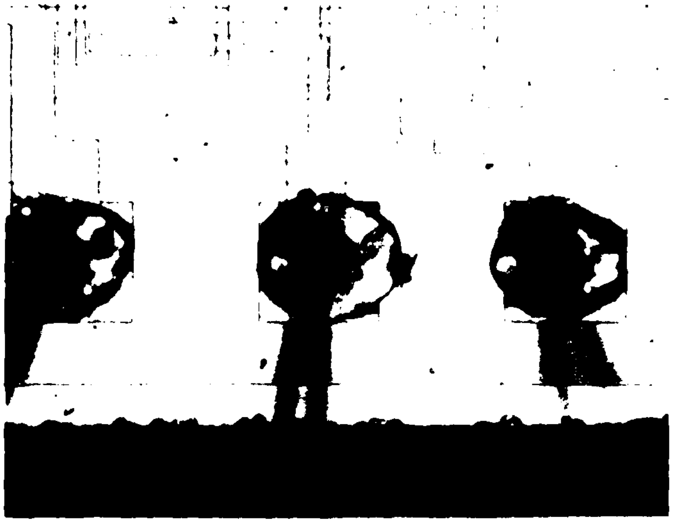


PHOTO 2 SN 065 750X

THIS SCANNING ELECTRON MICROPHOTOGRAPH (SEM) SHOWS IN GREATER DETAIL THESE FORMATIONS.

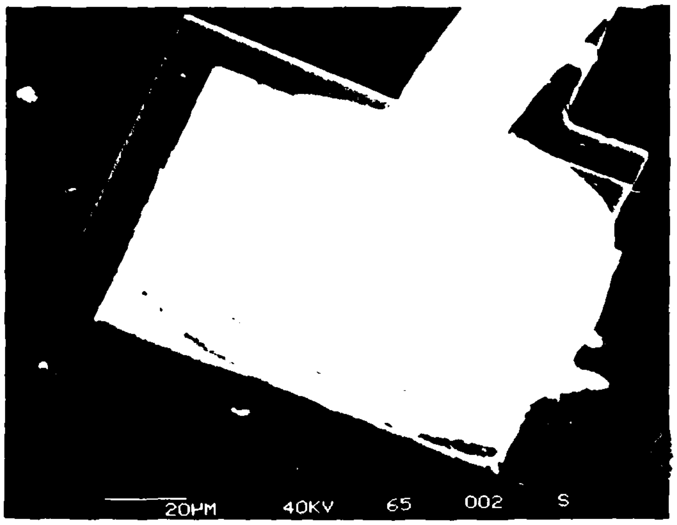
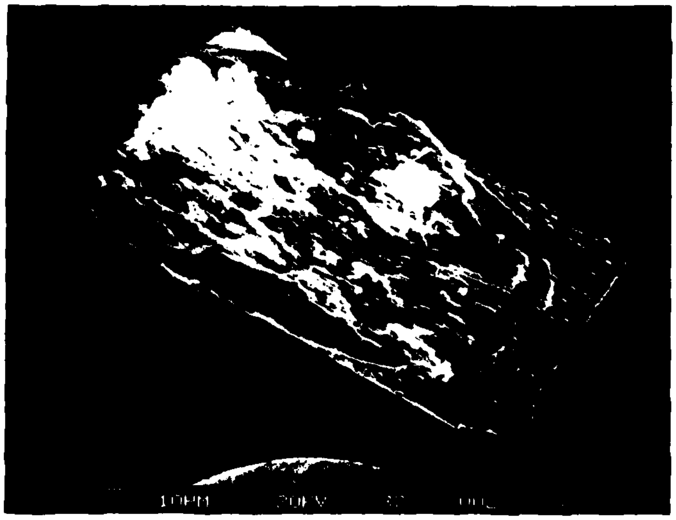


PHOTO 3 SN 037 800X

THIS SEM. VIEW SHOWS A BOND BALL HAD SEPARATED FROM ITS BOND PAD DURING TESTING. NOTICE THE REMAINING INTERMETALLIC FORMATION.



APPENDIX TO: LAR # 00124 AND 00123 PAGE 2 OF 2

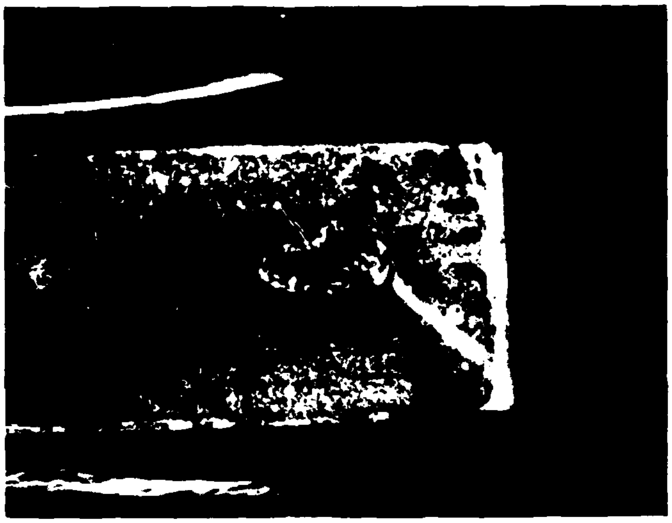


PHOTO 4 SN 037 104X

THIS IS A VISIBLE LIGHT MICROPHOTOGRAPH OF THE GOLD WIRE TO ALUMINUM PLATED LEAD POST BOND, TYPICAL OF THE GLASS FRIT SEALED CERDIPS.

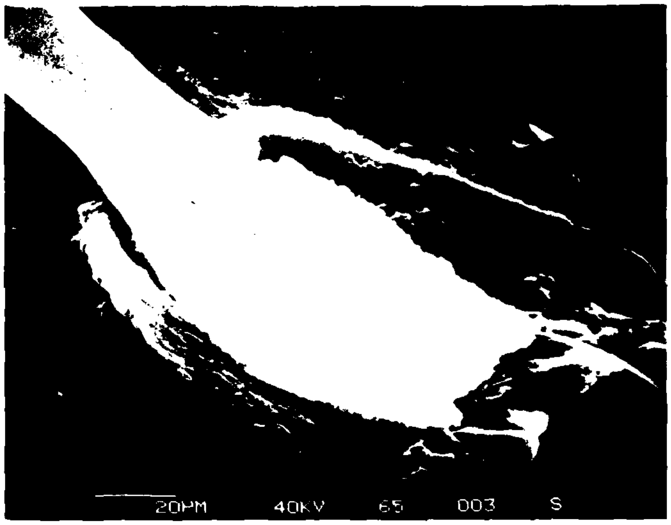


PHOTO 5 SN 065 700X

THIS IS AN S.E.M. PHOTO OF THE SAME TYPE OF BOND. THE HEEL AND FOOT ARE NO LONGER CONTINUOUS. NOTICE THE INTERMETALLIC FORMATIONS UNDER THE HEEL, ALSO.

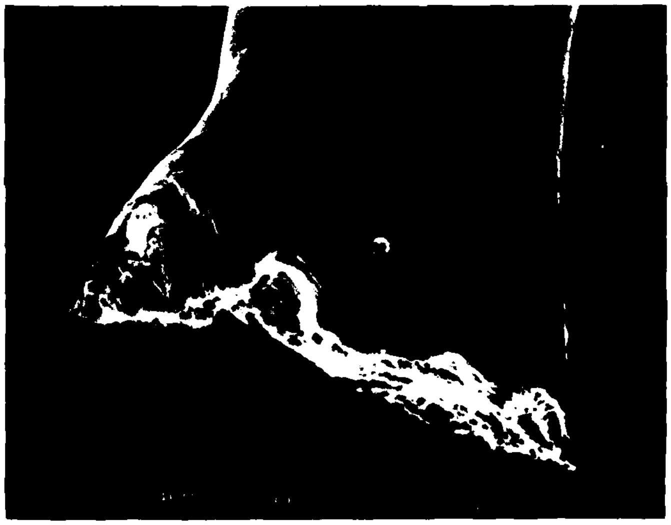


PHOTO 6 SN 037 2000X

THIS IS A HIGH RESOLUTION S.E.M. PHOTO OF THE END OF ONE OF THE BOND WIRES WHICH FAILED DURING TEST.

MARTIN MARIETTA

PHYSICS OF FAILURE LABORATORY
ANALYSIS REPORT

PAGE 1 OF 1

ANALYSIS NO. LAR# 00125

PROJECT QA-LSI

SOURCE DOC. NO. NA

PART NAME INTEGRATED CIRCUIT

MODEL NO. SB-40 S/N DATE CODE 054 - 8011

DRAWING NO. NA

SUPPLIER MARTIN MARIETTA MEC

ORIGIN OF FAILURE NA

FAILURE CODE ☐☐ ☐☐ ☐☐

REMARKS:

VERBAL REPORT TO L. MIRTH x3261

DATE: MAY 1, 1980

THIS SHORT FORM REPORT SUMMARIZES THE (1) HISTORY, (2) ANALYSIS PROCEDURE, (3) CONCLUSION, CAUSE (4) RECOMMENDATIONS.

HISTORY:

THIS DEVICE WAS SUBMITTED FOR DECAPPING AND INTERNAL VISUAL EXAMINATION AFTER HAVING BEEN SUBJECTED TO SCREENING AND QUALIFICATION TESTS.

EXAMINATION:

VISUAL EXAMINATION OF THE DIE CAVITY WAS PERFORMED IN ACCORDANCE WITH MIL-STD 883 METHODS USING LIGHT OPTICAL MICROSCOPES HAVING MAGNIFICATIONS FROM 10X TO 250X AND BRIGHT FIELD AND DARK FIELD ILLUMINATION.

RESULTS:

THE DIE CAVITY WAS CLEAN AND INTERNAL COMPONENTS WERE WELL POSITIONED. GOLD BALL ULTRASONIC BONDING WAS USED FOR ALL CONNECTIONS. THE DIE SURFACE CONTAINED MANY ATTACHED ORGANIC PARTICLES.

THERE WERE NO INDICATIONS OF MECHANICAL DAMAGE OR CORROSION.

PHOTO 1 10X

OVERALL VIEW

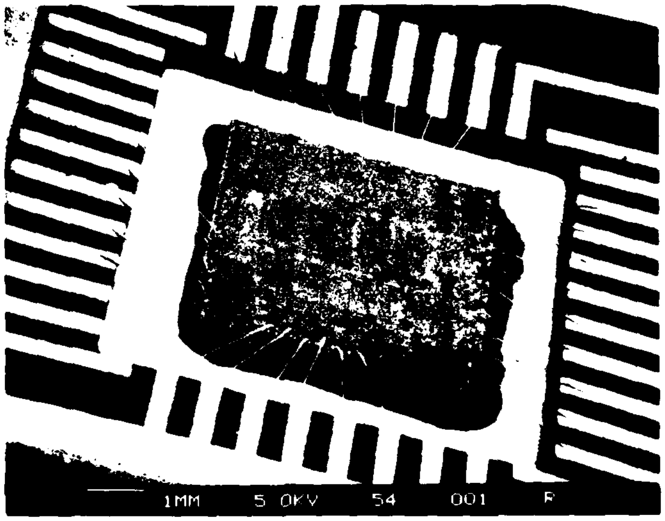
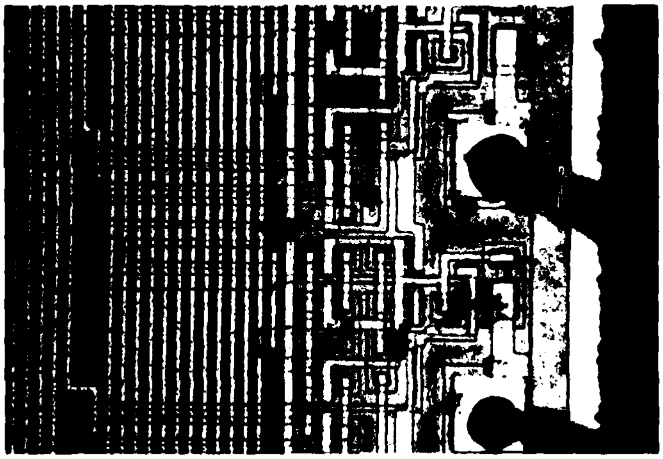


PHOTO 2 128X

SURFACE PARTICLES



CORRECTIVE ACTION RECOMMENDED

SUPPLIER ______

MFG ______

TEST ______

ENG ______

OTHER ______

DATE COMPLETED MAY 5 1980

ANALYSIS ENGR P. E. Zigler x3046

[illegible] ENGR Lee Mirth

APPROVALS

SAMPLE DISPOSITION

RETAINED ___ RETURNED X

Form Mar70 D-1672

MARTIN MARIETTA

PHYSICS OF FAILURE LABORATORY ANALYSIS REPORT

THIS SHORT FORM REPORT SUMMARIZES THE (1) HISTORY, (2) ANALYSIS PROCEDURE, (3) CONCLUSION (CAUSE), (4) RECOMMENDATIONS.

HISTORY:

THIS DEVICE WAS SUBMITTED FOR DECAPPING AND INTERNAL VISUAL EXAMINATION AFTER HAVING BEEN EXPOSED TO SCREENING AND QUALIFICATION TESTS.

EXAMINATION:

VISUAL EXAMINATION OF THE DIE CAVITY WAS PERFORMED IN ACCORDANCE WITH MIL-STD 883 METHODS AND USING LIGHT OPTICAL MICROSCOPES FROM 10X TO 250X MAGNIFICATIONS AND BOTH BRIGHT FIELD AND DARK FIELD ILLUMINATION.

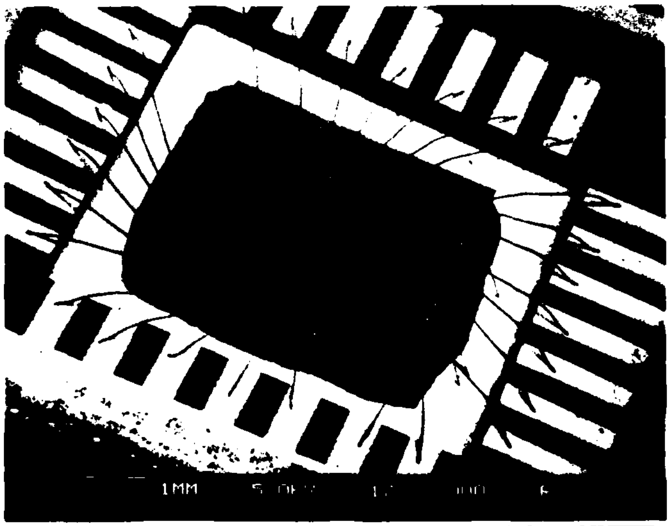
RESULTS:

THE DIE CAVITY WAS CLEAN AND INTERNAL COMPONENTS WERE WELL POSITIONED. ALUMINUM ULTRASONIC WIRE BONDING WAS USED FOR ALL BUT FOUR CONNECTIONS. GOLD BALL BONDING WAS USED FOR ALL FOUR SUBSTRATE CONNECTIONS.

THERE WERE NO INDICATIONS OF MECHANICAL DAMAGE OR CORROSION.

PHOTO 1 10X

OVERALL DIE CAVITY



PAGE 1 OF 1

ANALYSIS NO: LAR-00126

PROJECT: QA-LSI

SOURCE DOC. NO: N A

PART NAME: INTEGRATED CIRCUIT

MODEL NO: SB-28

S N - DATE CODE: 017 - 8011

DRAWING NO.: N A

SUPPLIER: MARTIN MARIETTA MEC

ORIGIN OF FAILURE: NA

FAILURE CODE: ☐☐ ☐☐ ☐☐

REMARKS:

VERBAL REPORT

TO: L. MIRTH x3261

DATE: MAY 1, 1980

CORRECTIVE ACTION RECOMMENDED:

SUPPLIER ____________

MFG. ____________

TEST ____________

ENG. ____________

OTHER ____________

DATE COMPLETE: MAY 5 1980

ANALYSIS ENGR.: E. L. Zigler x3046

COMP. DES. ENGR.: Lee Mirth

APPROVALS:

SAMPLE DISPOSITION:

RETAINED ☐ RETURNED ☒

Form D-1672
Mar 70

MARTIN MARIETTA

PHYSICS OF FAILURE LABORATORY ANALYSIS REPORT

THIS SHORT FORM REPORT SUMMARIZES THE (1) HISTORY, (2) ANALYSIS PROCEDURE (3) CONCLUSION (CAUSE) (4) RECOMMENDATIONS.

HISTORY:

THIS DEVICE WAS SUBMITTED FOR DECAPPING AND INTERNAL VISUAL EXAMINATION AFTER HAVING BEEN SUBJECTED TO SCREENING AND QUALIFICATION TESTS. GP. A

EXAMINATION:

VISUAL EXAMINATION OF THE INTERNAL CAVITY WAS PERFORMED IN ACCORDANCE MIL-STD 883 METHODS USING LIGHT OPTICAL MICROSCOPES AT MAGNIFICATIONS FROM 10X TO 250X AND BOTH BRIGHT FIELD AND DARK FIELD ILLUMINATION.

RESULTS:

THE CHIP CAPACITOR WAS LOOSE INSIDE THE PACKAGE. THE EPOXY TO GOLD THIN FILM ADHESION FAILED AT BOTH ENDS. EXCEPT FOR DAMAGE DONE BY THE LOOSE CHIP CAPACITOR, THERE WERE NO SIGNS OF MECHANICAL DAMAGE OR CORROSION.

PHOTO 1 20X

CAPACITOR MOUNTING LOCATION

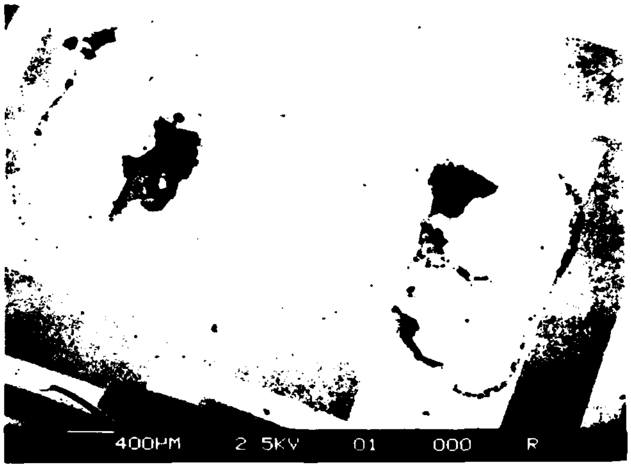
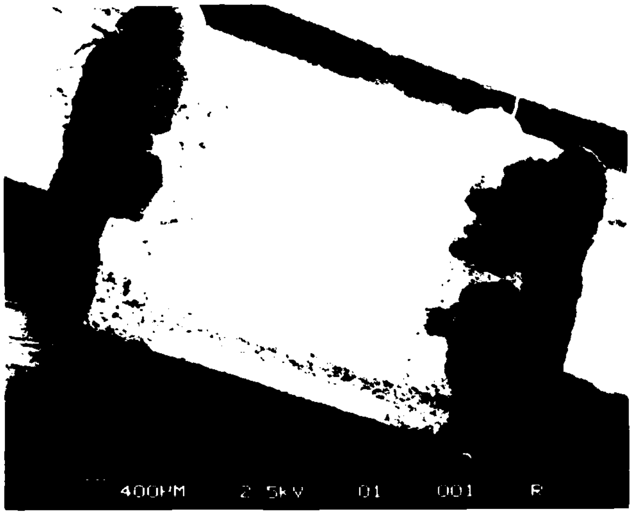


PHOTO 2 22X

CAPACITOR WITH EPOXY AT BOTH ENDS.



PAGE 1 OF 1

ANALYSIS NO LAR • 00127

PROJECT QA-LSI

SOURCE DOC. NO NA

PART NAME I.C. HYBRID

MODEL NO. H074 S/N - DATE CODE 001- NA

DRAWING NO. NA

SUPPLIER MARTIN MARIETTA MEC

ORIGIN OF FAILURE NA

FAILURE CODE ☐☐ ☐☐ ☐☐

REMARKS:

VERBAL REPORT TO: L. MIRTH X 3261

DATE: MAY 6, 1980

CORRECTIVE ACTION RECOMMENDED:

SUPPLIER ______

MFG ______

TEST ______

ENG ______

OTHER ______

DATE COMPLETE: MAY 8 1980

ANALYSIS ENGR. E. L. Zigler X 3046

COMP./DES. ENGR. Lee Mirth

APPROVALS:

SAMPLE DISPOSITION: RETAINED ☐ RETURNED ☒

Form D-1672 Mar70

MARTIN MARIETTA

PHYSICS OF FAILURE LABORATORY ANALYSIS REPORT

THIS SHORT FORM REPORT SUMMARIZES THE (1) HISTORY, (2) ANALYSIS PROCEDURE, (3) CONCLUSION (CAUSE) (4) RECOMMENDATIONS.

HISTORY:

THIS DEVICE WAS SUBMITTED FOR DECAPPING AND INTERNAL VISUAL EXAMINATION AFTER HAVING BEEN SUBJECTED TO SCREENING AND QUALIFICATION TESTS.

GPA

EXAMINATION:

VISUAL EXAMINATION OF THE INTERNAL CAVITY WAS PERFORMED IN ACCORDANCE WITH MIL-STD 883 METHODS USING LIGHT OPTICAL MICROSCOPES AT MAGNIFICATIONS FROM 10X TO 250X AND BOTH BRIGHT FIELD AND DARK FIELD ILLUMINATION.

RESULTS:

THE CHIP CAPACITOR AND THE DIODE CHIP WHICH HAD BEEN MOUNTED ADJACENT TO IT WERE BOTH LOOSE INSIDE THE PACKAGE. THE DIODE MOUNTING EPOXY SEPARATED FROM THE GOLD THIN FILM. THIS WAS ALSO THE CASE FOR ONE END OF THE CAPACITOR. THE OTHER END OF THE CAPACITOR SEPARATED BETWEEN THE CAPACITOR METALLIZATION AT THE EPOXY MOUNTING MATERIAL. (SEE PHOTOS 1-3)

MOST BOND WIRES WERE BENT INDICATING THAT THE CAPACITOR HAD MOVED AROUND THE PACKAGE. ALL BOND WIRING WAS ALUMINUM.

PAGE 1 OF 2

ANALYSIS NO. LAR# 00128

PROJECT QA-LSI

SOURCE DOC. NO. NA

PART NAME I.C. HYBRID

MODEL NO H074

S.N. - DATE CODE 044 - NA

DRAWING NO NA

SUPPLIER MARTIN MARIETTA MEC

ORIGIN OF FAILURE NA

FAILURE CODE ☐☐ ☐☐ ☐☐

REMARKS:

VERBAL REPORT

TO: L. MIRTH x 3261

DATE: MAY 6, 1980

CORRECTIVE ACTION RECOMMENDED:

SUPPLIER ____

MFG ____

TEST ____

ENG ____

OTHER ____

DATE COMPLETE: MAY 8, 1980

ANALYSIS ENGR. C. L. Zigler x3046

COMP. DES. ENGR. Lee Mirth

APPROVALS:

SAMPLE DISPOSITION:

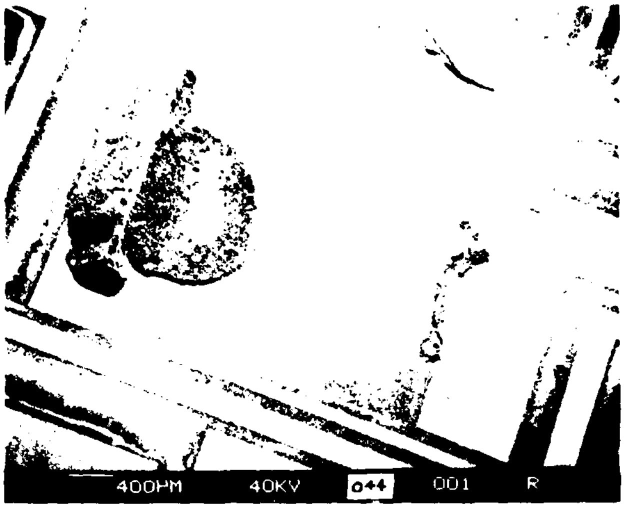
RETAINED ☐ RETURNED ☒

Form Mar70 D-1872

LAR# 00128 PAGE 2 OF 2

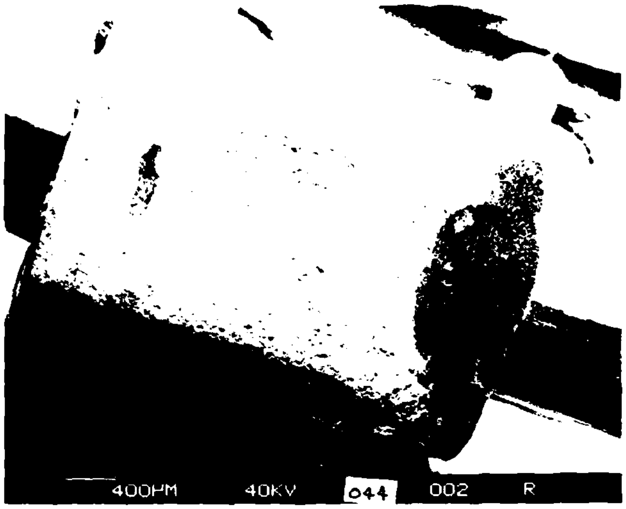
PHOTOGRAPH 1 16X

CHIP CAPACITOR MOUNTING LOCATION.


400PM
40KV
044
001
R

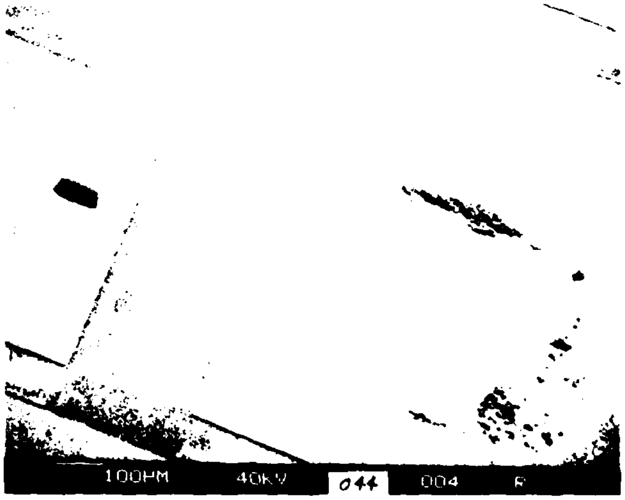
PHOTOGRAPH 2 21X

BOTTOM OF LOOSE CHIP CAPACITOR.


400PM
40KV
044
002
R

PHOTOGRAPH 3 80X

DIODE MOUNTING LOCATION.


100PM
40KV
044
004
R

MARTIN MARIETTA

PHYSICS OF FAILURE LABORATORY ANALYSIS REPORT

THIS SHORT FORM REPORT SUMMARIZES THE (1) HISTORY, (2) ANALYSIS PROCEDURE, (3) CONCLUSION (CAUSE), (4) RECOMMENDATIONS.

HISTORY:

THIS DEVICE WAS SUBMITTED FOR DECAPPING AND VISUAL EXAMINATION AFTER HAVING BEEN SUBJECTED TO SCREENING AND QUALIFICATION TESTS. GP A

EXAMINATION:

VISUAL EXAMINATION OF THE INTERNAL CAVITY WAS PERFORMED IN ACCORDANCE MIL-STD 883 METHODS USING LIGHT OPTICAL MICROSCOPES AT MAGNIFICATIONS FROM 10X TO 250X AND BOTH BRIGHT FIELD AND DARK FIELD ILLUMINATION.

RESULTS:

THE CHIP CAPACITOR WAS LOOSE INSIDE THE PACKAGE. BOND SEPARATION OCCURED AT THE GOLD THIN FILM AT ONE END AND AT THE CAPACITOR METALLIZATION ON THE OTHER END. (SEE PHOTOS 1+2)

THE INTERNAL WIRING WAS GOLD ULTRASONIC BALL BONDING. ONE GOLD BALL WAS LIFTED FROM THE DIODE ADJACENT TO THE CAPACITOR (SEE PHOTOS 2+3). THE DIODE METALLIZATION APPEARED TO BE LIFTED AND TORN ADJACENT TO THE BOND AREA. THE BOND IMPRINT INDICATED LESS THAN 20% OF THE BOND AREA WAS AN EFFECTIVE METALLURGICAL BOND.

THERE WERE NO INDICATIONS OF CORROSION OR OTHER MECHANICAL DAMAGE.

PAGE 1 OF 2

ANALYSIS NO. LAR# 00129

PROJECT QA-LSI

SOURCE DOC. NO. NA

PART NAME I.C. HYBRID

MODEL NO. H074 S/N - DATE CODE 015- NA

DRAWING NO. NA

SUPPLIER MARTIN MARIETTA MEC

ORIGIN OF FAILURE NA

FAILURE CODE ☐☐ ☐☐ ☐☐

REMARKS:

VERBAL REPORT TO: L. MIRTH X3261

DATE: MAY 6, 1980

CORRECTIVE ACTION RECOMMENDED:

SUPPLIER ____

MFG. ____

TEST ____

ENG. ____

OTHER ____

DATE COMPLETE: MAY 8, 1980

ANALYSIS ENGR. E. S. Zigler x3046

COMP./DES. ENGR. Lee Mirth

APPROVALS:

SAMPLE DISPOSITION:

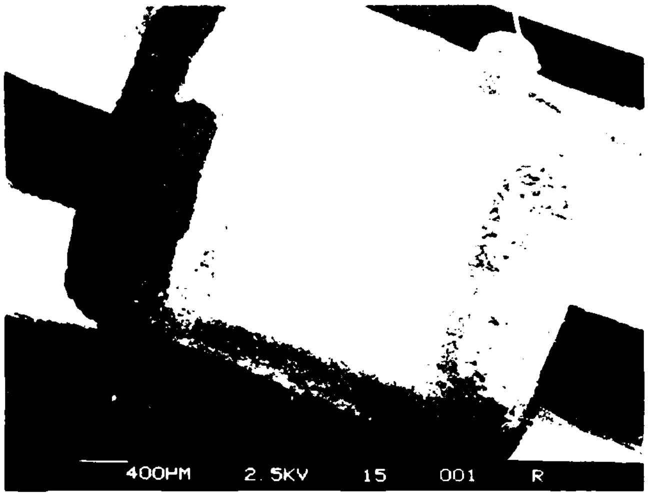
RETAINED ☐ RETURNED ☒

Form Mar70 D-1672

LAR# 00129　　PAGE 2 OF 2

PHOTOGRAPH 1　　20X

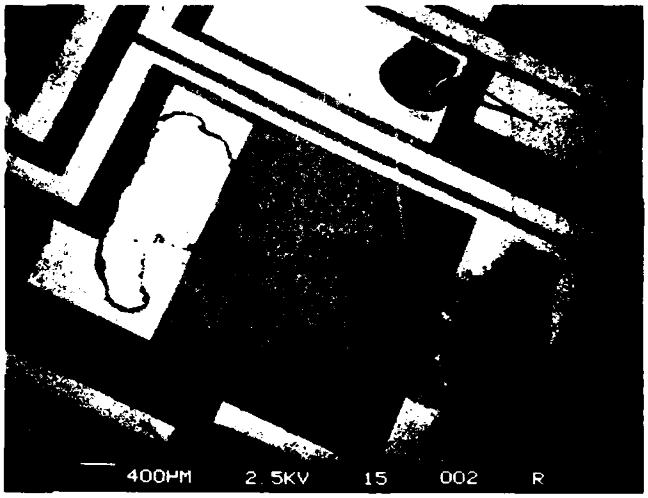
BOTTOM SIDE OF LOOSE CHIP CAPACITOR


400µM 2.5KV 15 001 R

PHOTOGRAPH 2　　15X

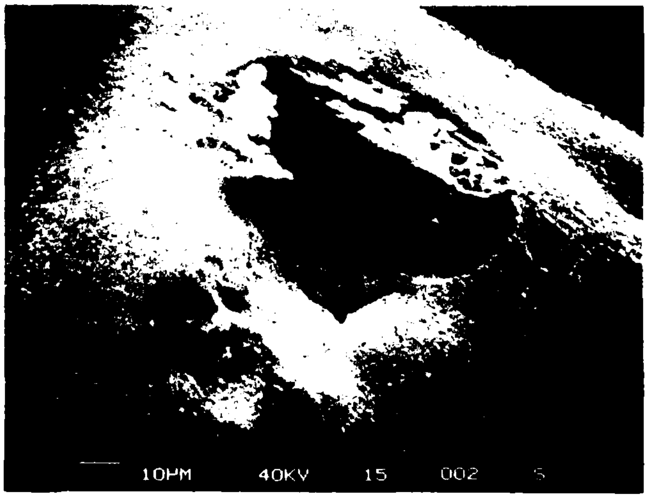
ORIGINAL MOUNTING SITE OF CAPACITOR

NOTE LIFTED GOLD BOND BALL ON DIODE CHIP


400µM 2.5KV 15 002 R

PHOTOGRAPH 3　　700X

METALLIZATION WHERE BOND BALL HAD BEEN ATTACHED SHOWS <20% EFFECTIVE BOND AREA AS WELL AS TORN WINDOW METALLIZATION.


10µM 40KV 15 002 S

MARTIN MARIETTA

PHYSICS OF FAILURE LABORATORY ANALYSIS REPORT

PAGE 1 OF 2

ANALYSIS NO. LAR#00130

PROJECT QA-LSI

SOURCE DOC. NO. NA

PART NAME I.C. HYBRID

MODEL NO. H074 S/N - DATE CODE 028-NA

DRAWING NO. NA

SUPPLIER MARTIN MARIETTA MEC

ORIGIN OF FAILURE NA

FAILURE CODE ☐☐ ☐☐ ☐☐

REMARKS:

THIS SHORT FORM REPORT SUMMARIZES THE (1) HISTORY, (2) ANALYSIS PROCEDURE, (3) CONCLUSION (CAUSE), (4) RECOMMENDATIONS.

HISTORY:

THIS DEVICE WAS SUBMITTED FOR DECAPPING AND INTERNAL VISUAL EXAMINATION AFTER HAVING BEEN SUBJECTED TO SCREENING AND QUALIFICATION TESTS. GY A

EXAMINATION:

VISUAL EXAMINATION OF THE INTERNAL CAVITY WAS PERFORMED IN ACCORDANCE WITH MIL-STD 883 METHODS USING LIGHT OPTICAL MICROSCOPES AT MAGNIFICATIONS FROM 10X TO 250X AND BOTH BRIGHT FIELD AND DARK FIELD LIGHTING.

RESULTS:

THE CHIP CAPACITOR MOUNTING WAS STILL INTACT AS SHOWN IN PHOTO 1. THE BASE BOND WIRE WAS GONE FROM THE TRANSISTOR CHIP. THE FOOT SEPARATED FROM THE BOND PAD DUE TO POOR LOCATION AS SHOWN IN PHOTOS 2 AND 3.

ALL OTHER INTERNAL COMPONENTS WERE IN GOOD CONDITION.

THERE WERE NO INDICATIONS OF CORROSION.

VERBAL REPORT
TO: L. MIRTH X3261

DATE: MAY 6, 1980

CORRECTIVE ACTION RECOMMENDED:

SUPPLIER ______

MFG. ______

TEST ______

ENG. ______

OTHER ______

DATE COMPLETE: MAY 8, 1980

ANALYSIS ENGR. E. L. Zigler X3046

COMP./DES. ENGR. Lee Mirth

APPROVALS:

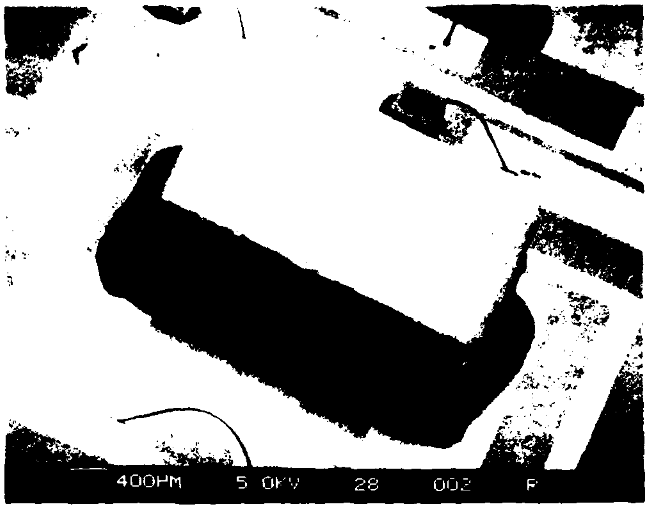
SAMPLE DISPOSITION:
RETAINED ☐ RETURNED ☒

Form Mar70 D-1672

LAR#00130 PAGE 2 OF 2

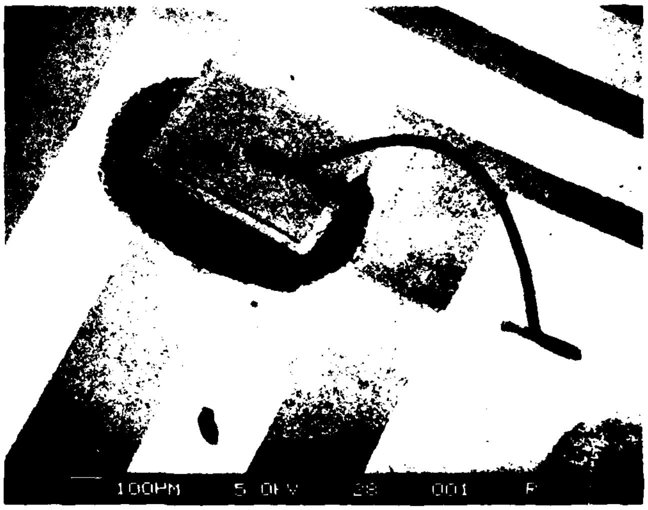
PHOTOGRAPH 1 18X

CHIP CAPACITOR WHICH SURVIVED TESTING.


400PM
5.0KV
28
002
P

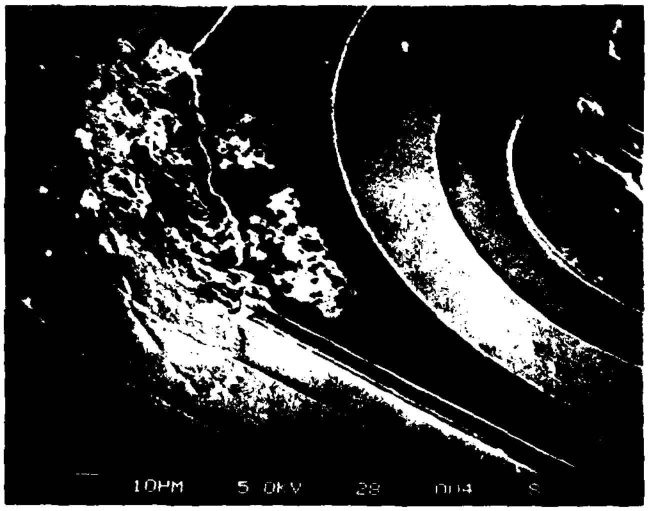
PHOTOGRAPH 2 65X

BASE BOND WIRE LIFTED FROM TRANSISTOR.


100PM
5.0KV
28
001
P

PHOTOGRAPH 3 550X

BOND FOOT IMPRINT SHOWS POOR LOCATION.


10PM
5.0KV
28
004
S

MARTIN MARIETTA

PHYSICS OF FAILURE LABORATORY ANALYSIS REPORT

THIS SHORT FORM REPORT SUMMARIZES THE (1) HISTORY, (2) ANALYSIS PROCEDURE, (3) CONCLUSION (CAUSE), (4) RECOMMENDATIONS.

HISTORY:

THIS DEVICE WAS SUBMITTED FOR DECAPPING AND INTERNAL EXAMINATION AFTER HAVING BEEN SUBJECTED TO SCREENING AND QUALIFICATION TESTS. GP. B

EXAMINATION:

VISUAL EXAMINATION OF THE INTERNAL CAVITY WAS PERFORMED IN ACCORDANCE WITH MIL-STD 883 METHODS USING LIGHT OPTICAL MICROSCOPES AT MAGNIFICATIONS FROM 10X TO 250X AND BOTH BRIGHT FIELD AND DARK FIELD ILLUMINATION.

RESULTS:

THE INTERNAL COMPONENTS WERE CLEAN AND WELL POSITIONED. ALL WIRING WAS ULTRASONICALLY BONDED ALUMINUM. THE CHIP CAPACITOR WAS STILL SECURED TO THE GOLD THIN FILM CONDUCTOR.

THERE WERE NO INDICATIONS OF MECHANICAL DAMAGE OR CORROSION.

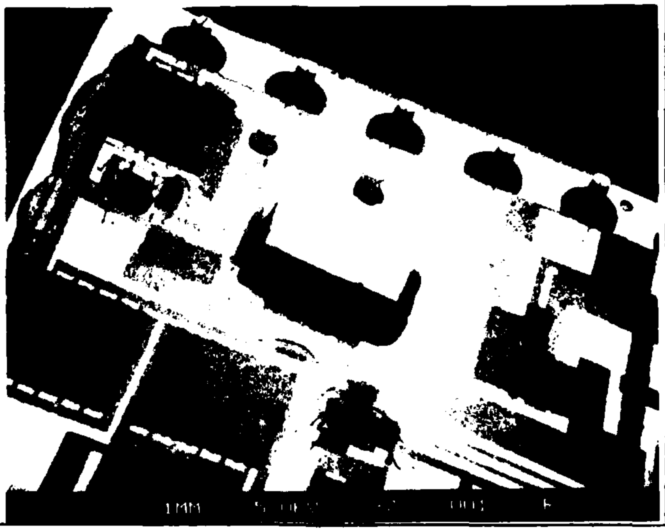


PHOTO 1 6.5X

OVERALL VIEW

PAGE 1 OF 1

ANALYSIS NO. LAR# 00131

PROJECT QA-LSI

SOURCE DOC. NO. NA

PART NAME I.C. HYBRID

MODEL NO. H074 S/N - DATE CODE 037- NA

DRAWING NO. NA

SUPPLIER MARTIN MARIETTA MEC

ORIGIN OF FAILURE NA

FAILURE CODE ☐☐ ☐☐ ☐☐

REMARKS:

VERBAL REPORT

TO: L. MIRTH X 3261

DATE: MAY 6 1980

CORRECTIVE ACTION RECOMMENDED:

SUPPLIER

MFG.

TEST

ENG.

OTHER

DATE COMPLETE: MAY 8, 1980

ANALYSIS ENGR E. L. Zigler X3046

COMP DES ENGR. Lee Mirth

APPROVALS:

SAMPLE DISPOSITION:

RETAINED ☐ RETURNED ☒

Form Mar70 D-1672

MARTIN MARIETTA

PHYSICS OF FAILURE LABORATORY ANALYSIS REPORT

THIS SHORT FORM REPORT SUMMARIZES THE (1) HISTORY, (2) ANALYSIS PROCEDURE (3) CONCLUSION/CAUSE (4) RECOMMENDATIONS.

HISTORY:

THIS DEVICE WAS SUBMITTED FOR DECAPPING AND INTERNAL VISUAL INSPECTION AFTER HAVING BEEN SUBJECTED TO SCREENING AND QUALIFICATION TESTS.

EXAMINATION:

VISUAL EXAMINATION OF THE INTERNAL CAVITY WAS PERFORMED IN ACCORDANCE WITH MIL-STD-883 METHODS USING LIGHT OPTICAL MICROSCOPES HAVING MAGNIFICATIONS FROM 10X TO 250X AND BOTH BRIGHT FIELD AND DARK FIELD ILLUMINATION.

RESULTS:

THE INTERNAL CAVITY WAS CLEAN, THE SEMICONDUCTOR DIE WAS WELL POSITIONED AND ALL BUT TWO OF THE GOLD BOND WIRES WERE IN GOOD CONDITION. THE Q105 AND Q115 INPUT BOND WIRES WERE MECHANICALLY DAMAGED (PHOTO 2) PRIOR TO LID SEAL. IN ADDITION THE CIRCUITRY AROUND THE Q67 INPUT BOND PAD WAS SERIOUSLY DAMAGED DURING THE WIRE BONDING PROCEDURE.

THERE WAS NO INDICATION OF CORROSION OR OTHER MECHANICAL DAMAGE.

PHOTO 1 9X

OVERALL VIEW

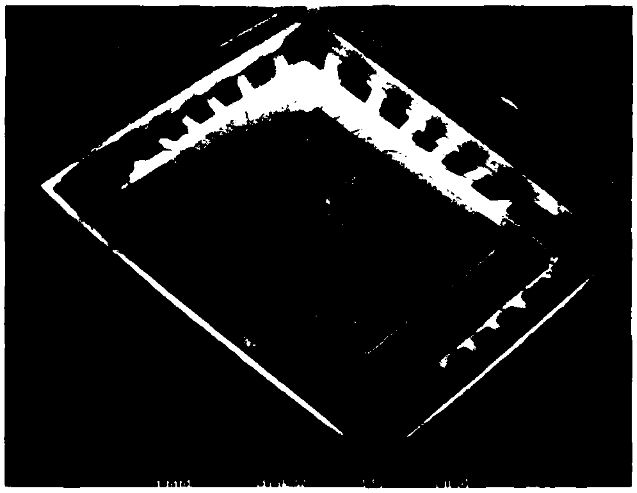


PHOTO 2 115X

DAMAGED BOND WIRES

PAGE 1 OF 1

ANALYSIS NO LAR# 00164

PROJECT QA-LSI

SOURCE DOC NO NA

PART NAME I.C. CHIP CARRIER

MODEL NO CM001 S N - DATE CODE 15G - NA

DRAWING NO NA

SUPPLIER MARTIN MARIETTA MEC

ORIGIN OF FAILURE NA

FAILURE CODE ☐☐ ☐☐ ☐☐

REMARKS:

VERBAL REPORT

TO: L. MIRTH X 3261

DATE: MAY 19, 1980

CORRECTIVE ACTION RECOMMENDED:

SUPPLIER ____

MFG ____

TEST ____

ENG ____

OTHER ____

DATE COMPLETE: MAY 19, 1980

ANALYSIS ENGR E. L. Zigler X3046

COMP. DES ENGR Lee Mirth

APPROVALS:

SAMPLE DISPOSITION:

RETAINED ☐ RETURNED ☒

Form D-1672 Mar70

MARTIN MARIETTA

PHYSICS OF FAILURE LABORATORY ANALYSIS REPORT

THIS SHORT FORM REPORT SUMMARIZES THE (1) HISTORY, (2) ANALYSIS PROCEDURE, (3) CONCLUSION (CAUSE) (4) RECOMMENDATIONS.

HISTORY:

THIS DEVICE WAS SUBMITTED FOR DECAPPING AND INTERNAL VISUAL EXAMINATION AFTER HAVING BEEN SUBJECTED TO SCREENING AND QUALIFICATION TESTS.

EXAMINATION:

VISUAL EXAMINATION OF THE INTERNAL CAVITY WAS PERFORMED IN ACCORDANCE WITH MIL-STD 883 METHODS USING LIGHT OPTICAL MICROSCOPES HAVING MAGNIFICATIONS FROM 10X TO 250X AND BOTH BRIGHT FIELD AND DARK FIELD ILLUMINATION.

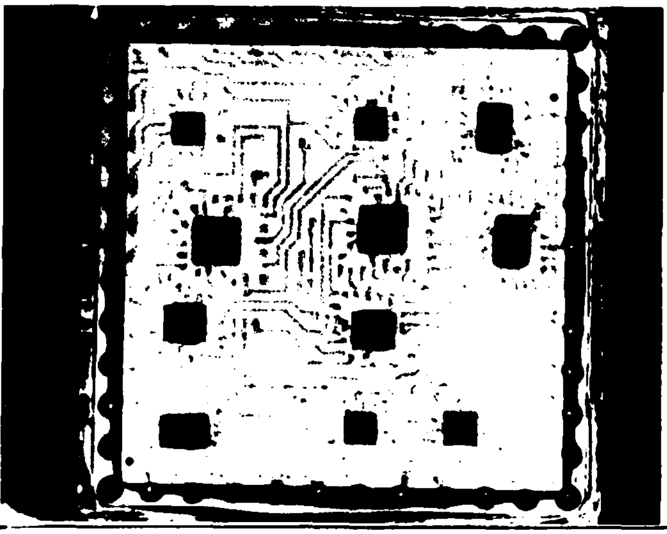
RESULTS:

THE INTERNAL COMPONENTS WERE CLEAN AND WELL POSITIONED. GOLD BALL BOND WIRING WAS USED THROUGHOUT. ALL SEMICONDUCTOR DEVICES AND WIRE BONDS WERE SECURE.

THERE WERE NO INDICATIONS OF CORROSION OR MECHANICAL DAMAGE.

PHOTO 1 2.7X

OVERALL VIEW



PAGE 1 OF 1

ANALYSIS NO: LAR# 00163

PROJECT: QA-LSI

SOURCE DOC NO: NA

PART NAME: I.C. HYBRID

MODEL NO: 72310026-9

S N - DATE CODE: 0026-NA

DRAWING NO.: NA

SUPPLIER: MARTIN MARIETTA MEC

ORIGIN OF FAILURE: NA

FAILURE CODE: ☐☐ ☐☐ ☐☐

REMARKS:

VERBAL REPORT TO: L. MIRTH X 3261

DATE: MAY 19, 1980

CORRECTIVE ACTION RECOMMENDED:

SUPPLIER ______

MFG ______

TEST ______

ENG ______

OTHER ______

DATE COMPLETE: MAY 19, 1980

ANALYSIS ENGR.: E. E. Zigler X 3046

COMP. DES. ENGR.: Lee Mirth

APPROVALS:

SAMPLE DISPOSITION:

RETAINED ☐ RETURNED ☒

Form D-1672
Mar70

MISSION
of
Rome Air Development Center

RADC plans and executes research, development, test and selected acquisition programs in support of Command, Control Communications and Intelligence (C^3I) activities. Technical and engineering support within areas of technical competence is provided to ESD Program Offices (POs) and other ESD elements. The principal technical mission areas are communications, electromagnetic guidance and control, surveillance of ground and aerospace objects, intelligence data collection and handling, information system technology, ionospheric propagation, solid state sciences, microwave physics and electronic reliability, maintainability and compatibility.

DATE
ILMED

82